

GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

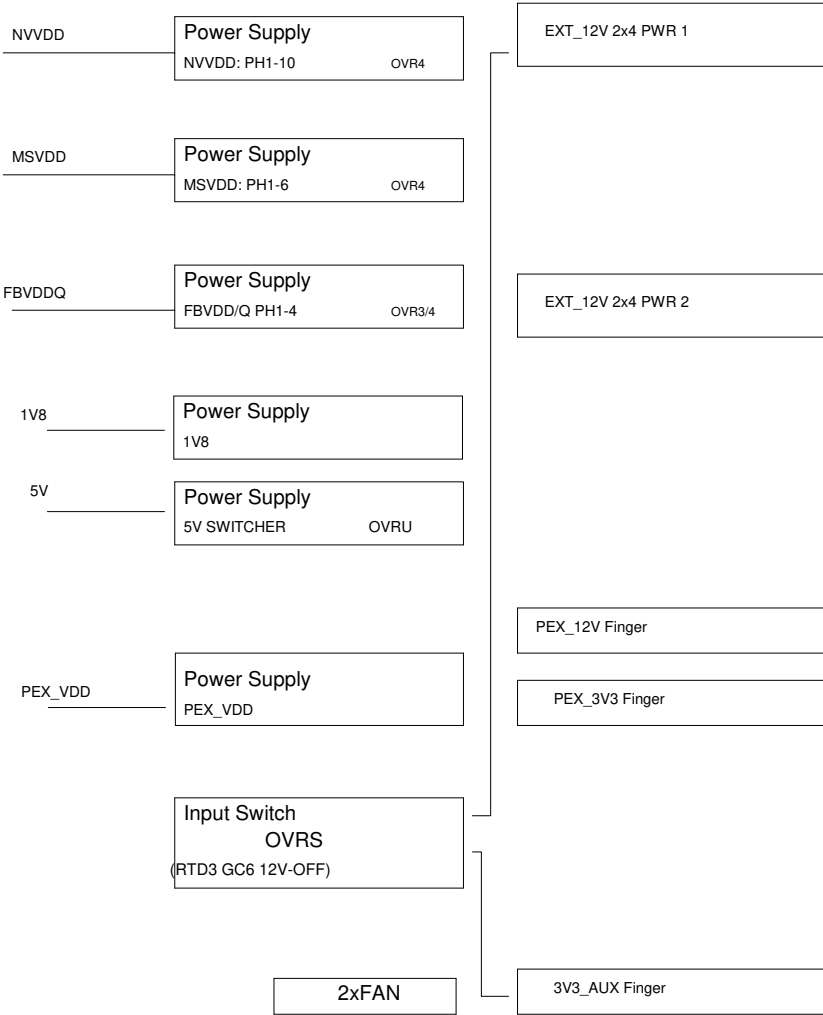
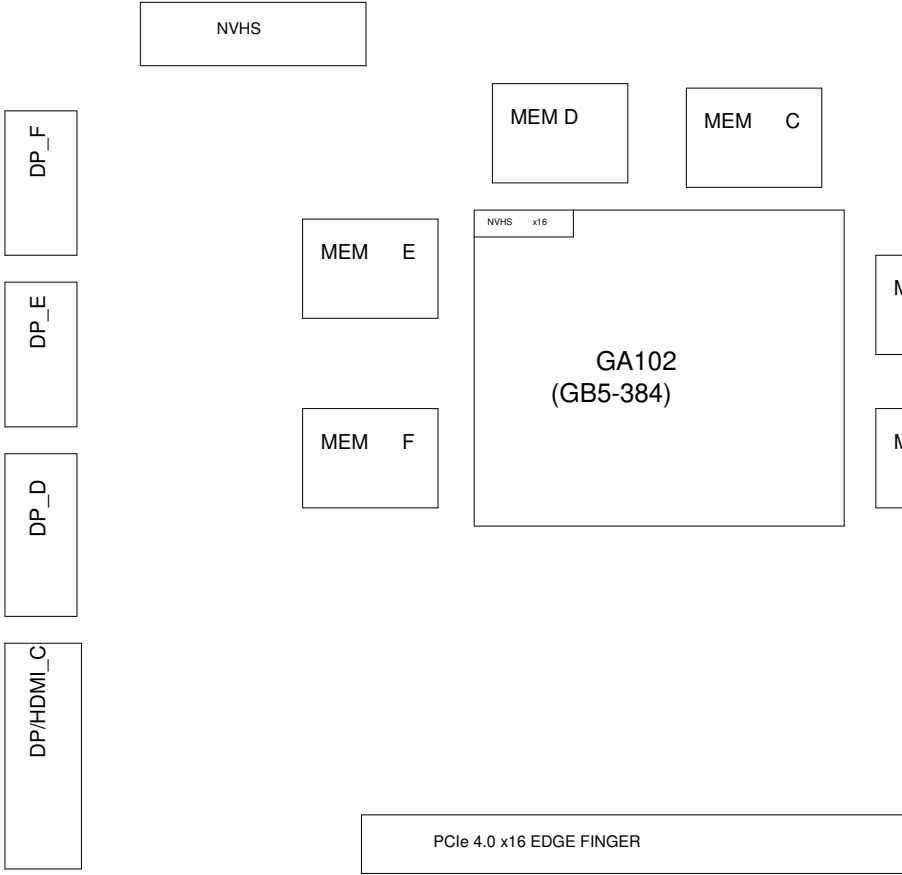
TABLE OF CONTENTS

| Page | Description |
|------|------------------------------|
| 1 | Table of Contents |
| 2 | BLOCK DIAGRAM |
| 3 | PCI EXPRESS |
| 4 | MEMORY: GPU PARTITION A/B |
| 5 | MEMORY: FBA PARTITION[31:0] |
| 6 | MEMORY: FBA PARTITION[63:32] |
| 7 | MEMORY: FBB PARTITION[31:0] |
| 8 | MEMORY: FBB PARTITION[63:31] |
| 9 | MEMORY: GPU PARTITION C/D |
| 10 | MEMORY: FBC PARTITION[31:0] |
| 11 | MEMORY: FBC PARTITION[63:32] |
| 12 | MEMORY: FBD PARTITION[31:0] |
| 13 | MEMORY: FBD PARTITION[63:32] |
| 14 | MEMORY: GPU PARTITION E/F |
| 15 | MEMORY: FBE PARTITION[31:0] |
| 16 | MEMORY: FBE PARTITION[63:32] |
| 17 | MEMORY: FBF PARTITION[31:0] |
| 18 | MEMORY: FBF PARTITION[63:32] |
| 19 | GPU GND, RFUs & RSVD |
| 20 | GPU POWERS |
| 21 | GPU: NVVDD DECOUPLING |
| 22 | GPU: FBVDD DECOUPLING |
| 23 | GPU: MSVDD DECOUPLING |
| 24 | BLANK |
| 25 | NVHS x16 |

| Page | Description |
|------|---------------------------|
| 26 | MISC: THERMAL, JTAG, GPIO |
| 27 | IFPA UNUSED, IFPB UNUSED |
| 28 | IFPE DP |
| 29 | IFPD DP |
| 30 | IFPC HDMI/DP |
| 31 | IFPF DP |
| 32 | MISC. ROM, STRAPS |
| 33 | MISC. XTAL, PLL |
| 34 | PS: 5V |
| 35 | PS: PEX_DVDD and 1V8 |
| 36 | BLANK |
| 37 | PS: FBVDD Controller OVR3 |
| 38 | PS: FBVDDQ OVR4 |
| 39 | PS: FBVDD PH1 |
| 40 | PS: FBVDD PH3 |
| 41 | PS: FBVDD PH2 |
| 42 | PS: FBVDD PH4 |
| 43 | PS: FBVDD OUTPUT CAP |
| 44 | PS: MSVDD CONTROLLER |
| 45 | PS: MSVDD PH1 |
| 46 | PS: MSVDD PH2 |
| 47 | PS: MSVDD PH3 and PH5 |
| 48 | PS: MSVDD PH4 and PH6 |
| 49 | PS: MSVDD OUTPUT CAP(TOP) |
| 50 | BLANK |

| Page | Description |
|------|--|
| 51 | PS: NVVDD Controller_OVR8 |
| 52 | PS: NVVDD PH1 (PWM1) |
| 53 | PS: NVVDD PH2 (PWM6) |
| 54 | PS: NVVDD PH3 (PWM3) and PH4 (PWM3) |
| 55 | PS: NVVDD PH5 (PWM7) and PH7 (PWM8) |
| 56 | PS: NVVDD PH6 (PWM7) |
| 57 | PS: NVVDD PH8(PWM5) and PH9(PWM2) |
| 58 | PS: NVVDD PH10 (PWM4) |
| 59 | Colayout Notes |
| 60 | BLANK |
| 61 | PS: NVVDD OUTPUT CAP(TOP) |
| 62 | BLANK |
| 63 | PS: INPUT SWITCH RTD3 |
| 64 | BLANK |
| 65 | PS: INPUTS, FILTERING, and, MONITORING |
| 66 | PS: HOT UNPLUG |
| 67 | PS: Discrete Power Steering |
| 68 | PS: PREFILTER |
| 69 | PS: PREFILTER B |
| 70 | Sequence: 5V, 1V8, 3V3_SEQ |
| 71 | Sequence: NV, PEX, FB EN |
| 72 | Sequence: 3V3 MONITOR |
| 73 | Sequence: MISC |
| 74 | MISC: LED & FAN |
| 75 | RGBW LED REF |

Block Diagram



MEMORY: GPU Partition A/B

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ASSEMBLY DESCRIPTION
MEMORY: GPU PARTITION A/B

GIGABYTE

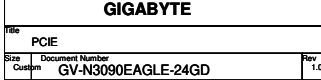
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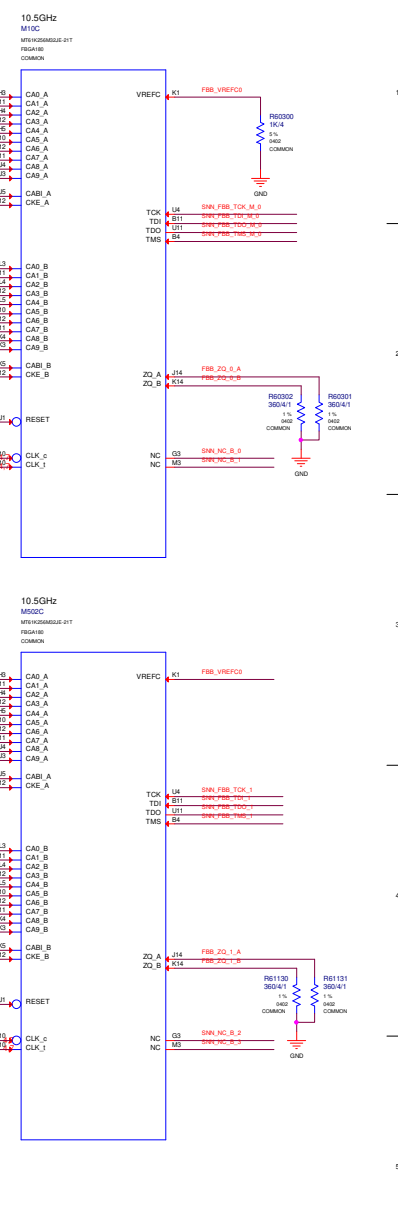
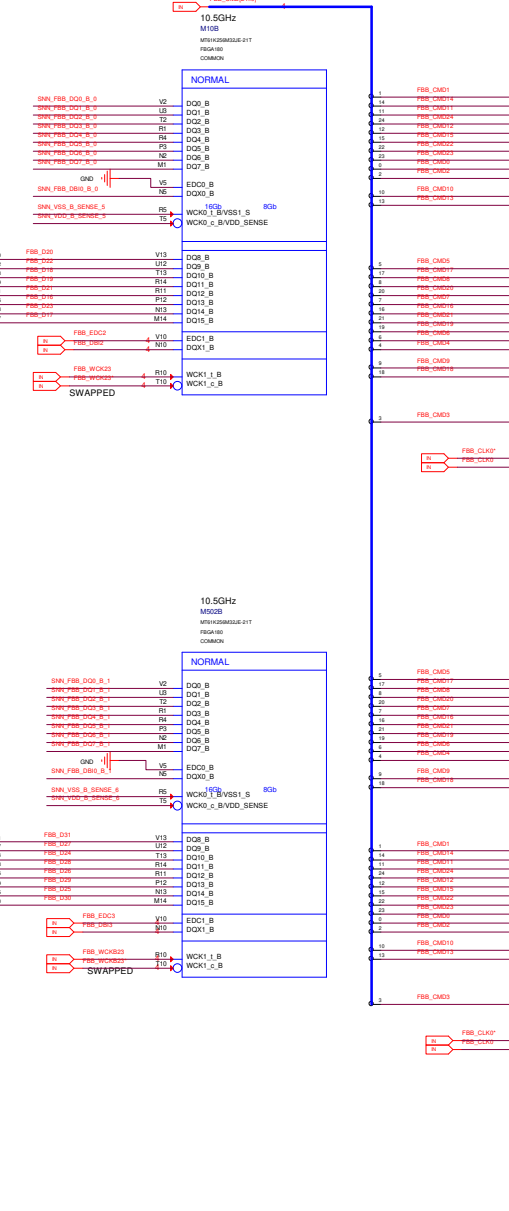
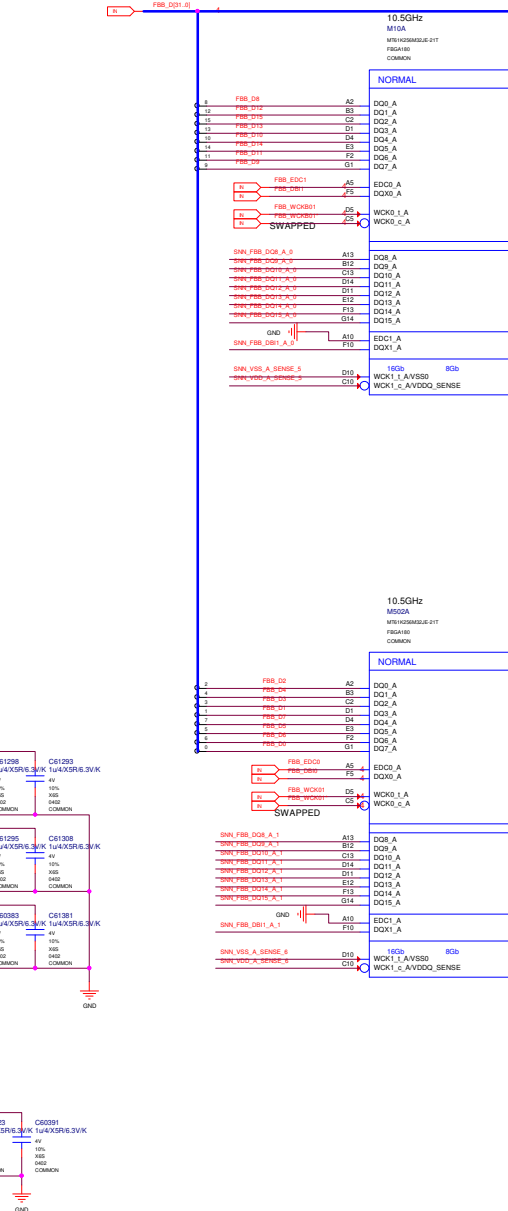
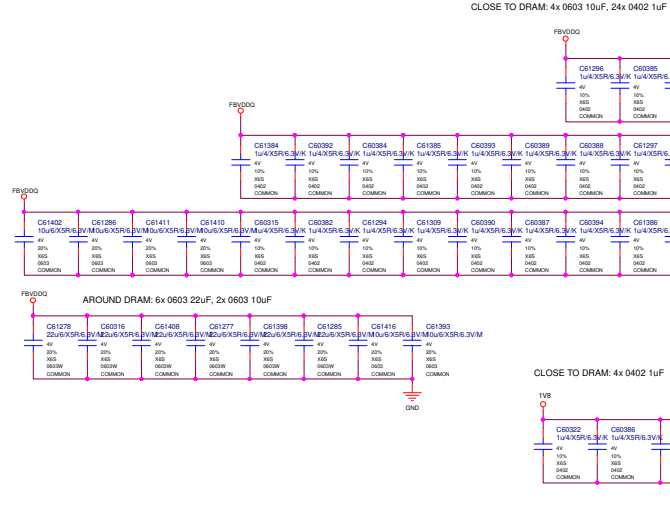
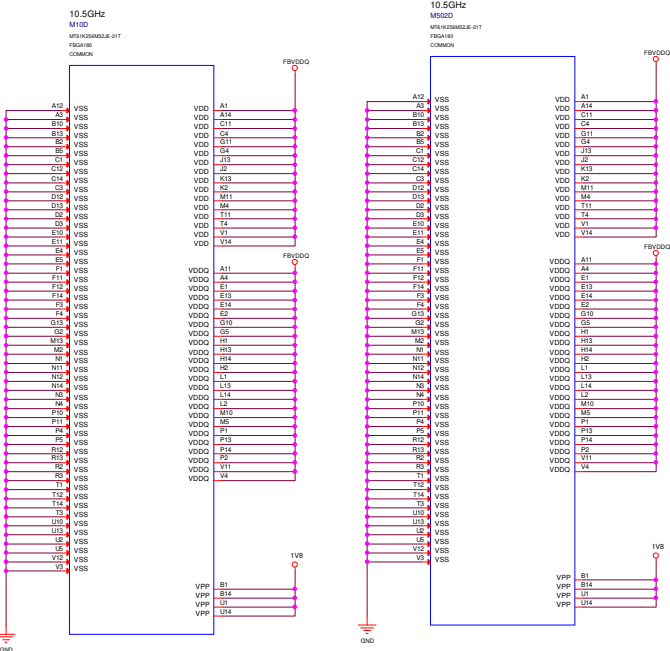
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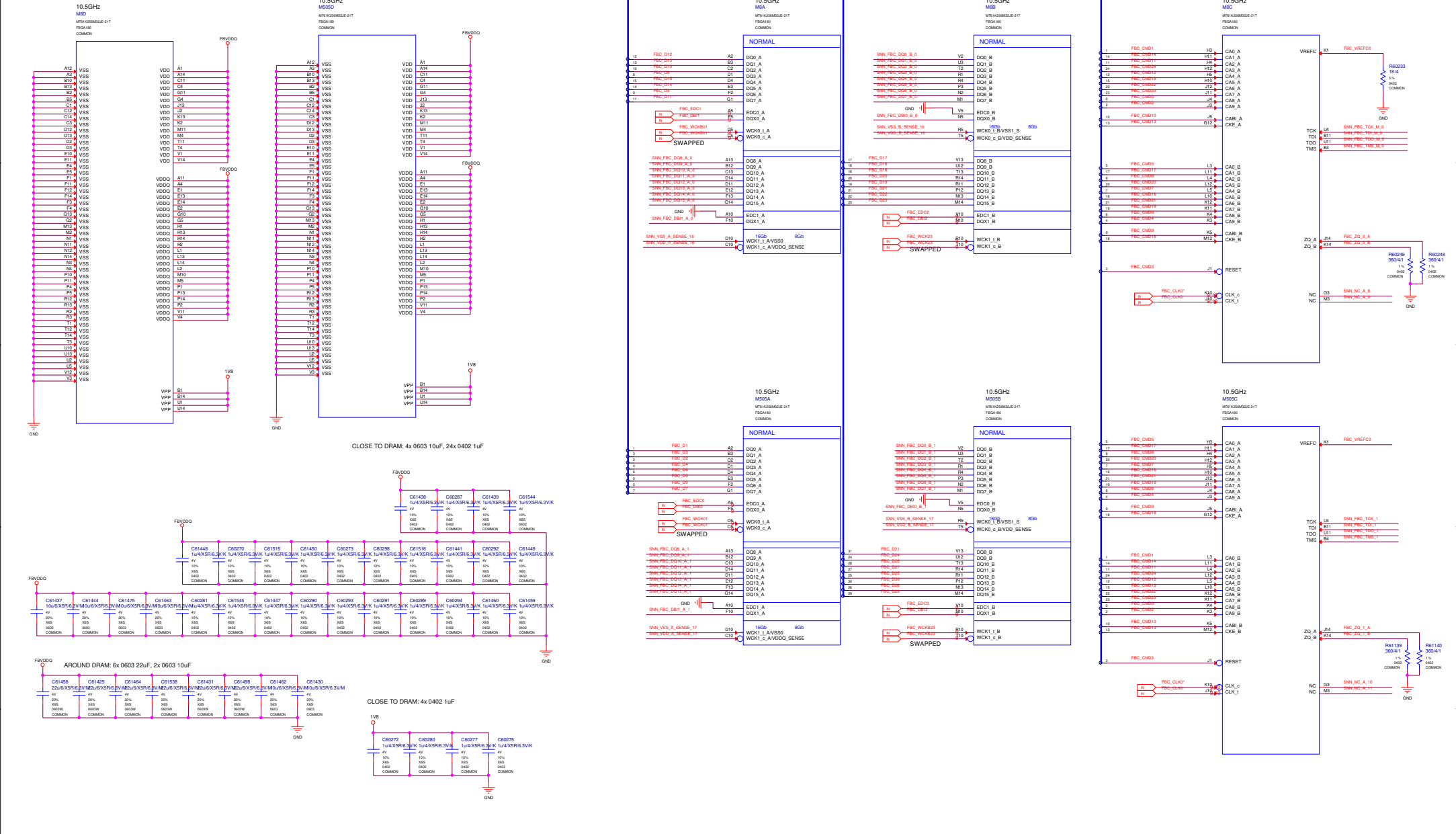
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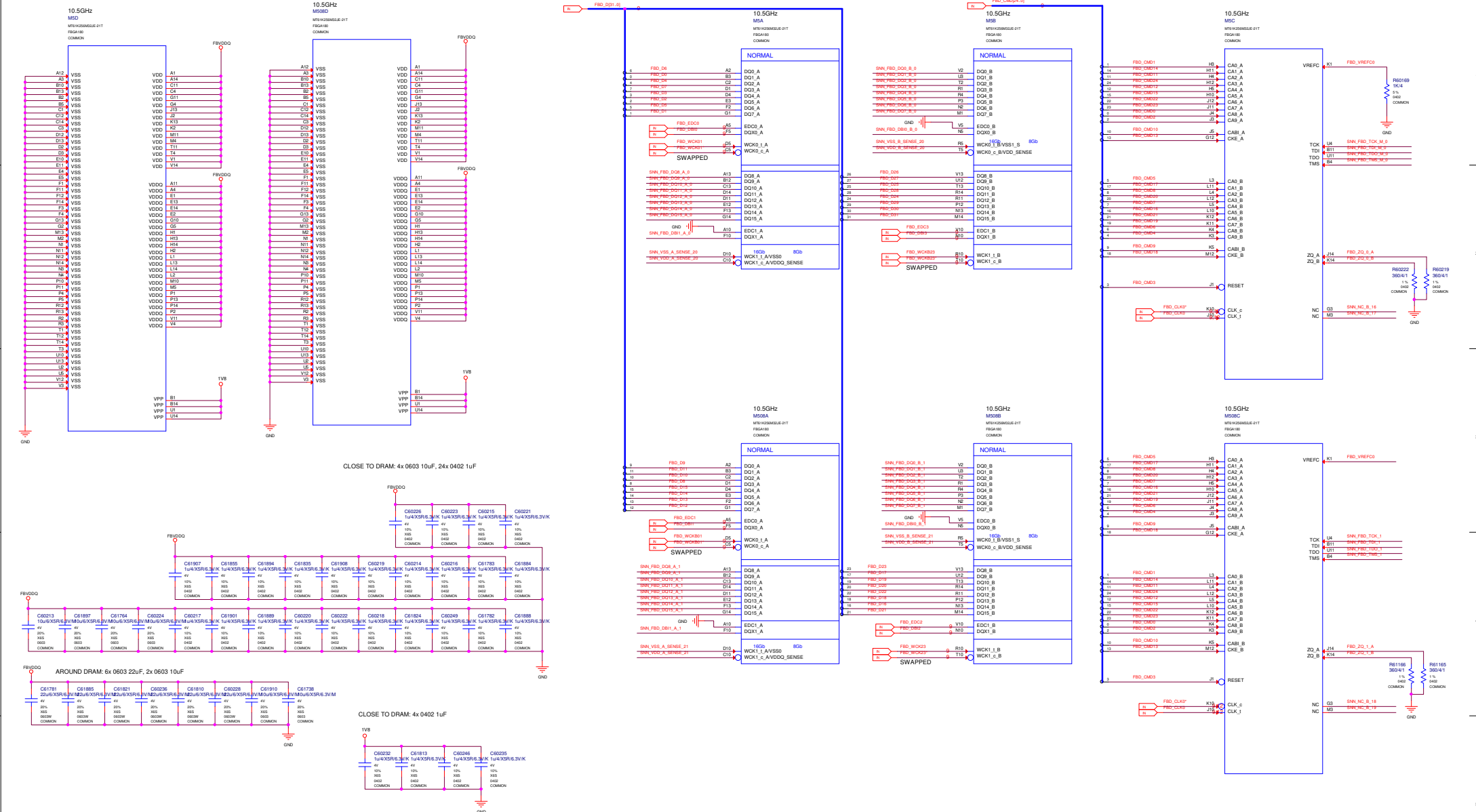
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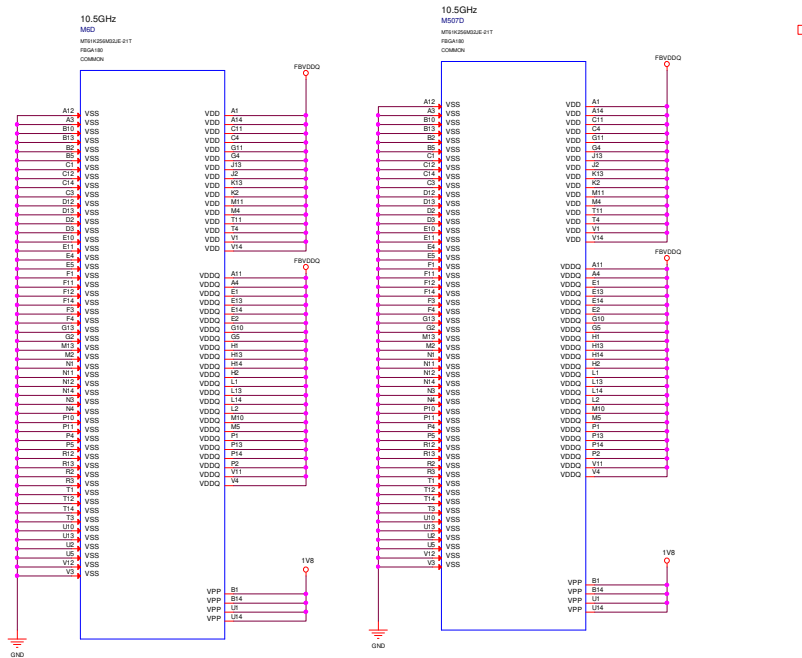
Date: Wednesday, September 30, 2020 Sheet 4 of 82



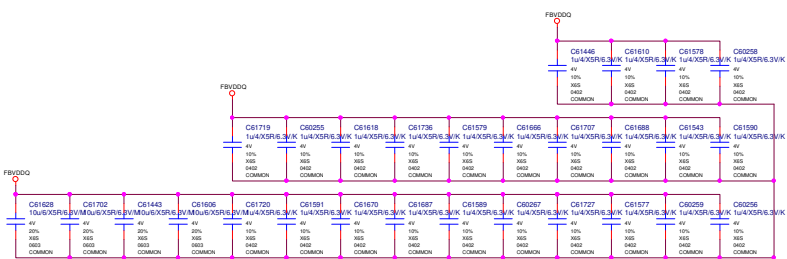




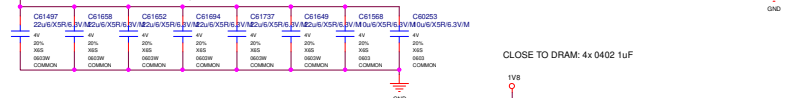




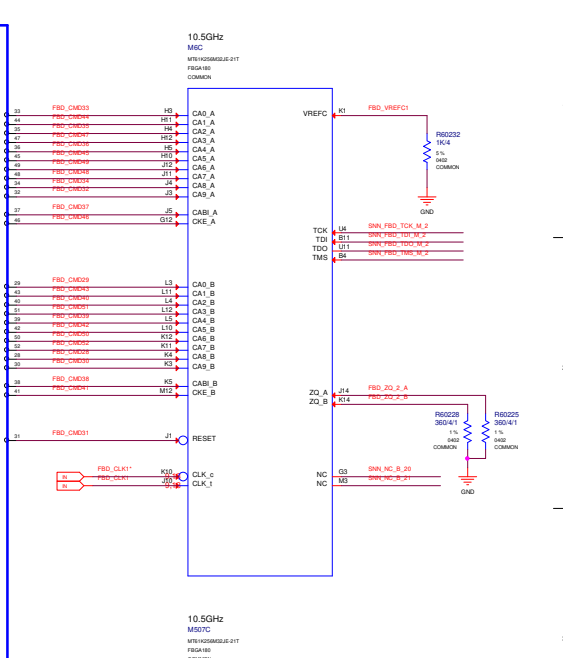
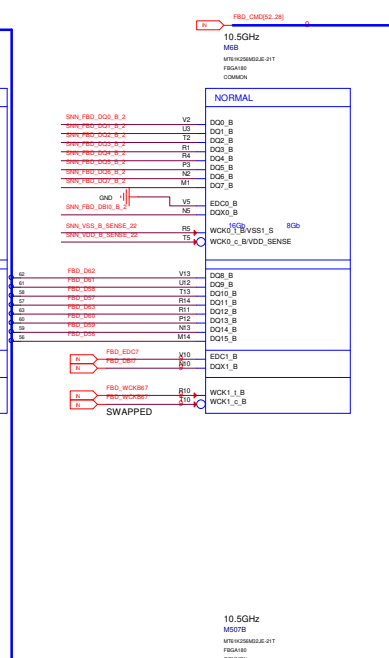
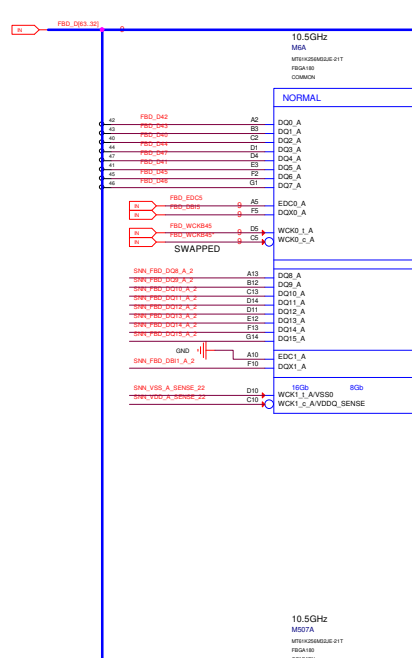
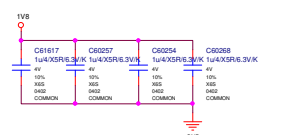
CLOSE TO DRAM: 4x 0603 100F, 24x 0402 1uF



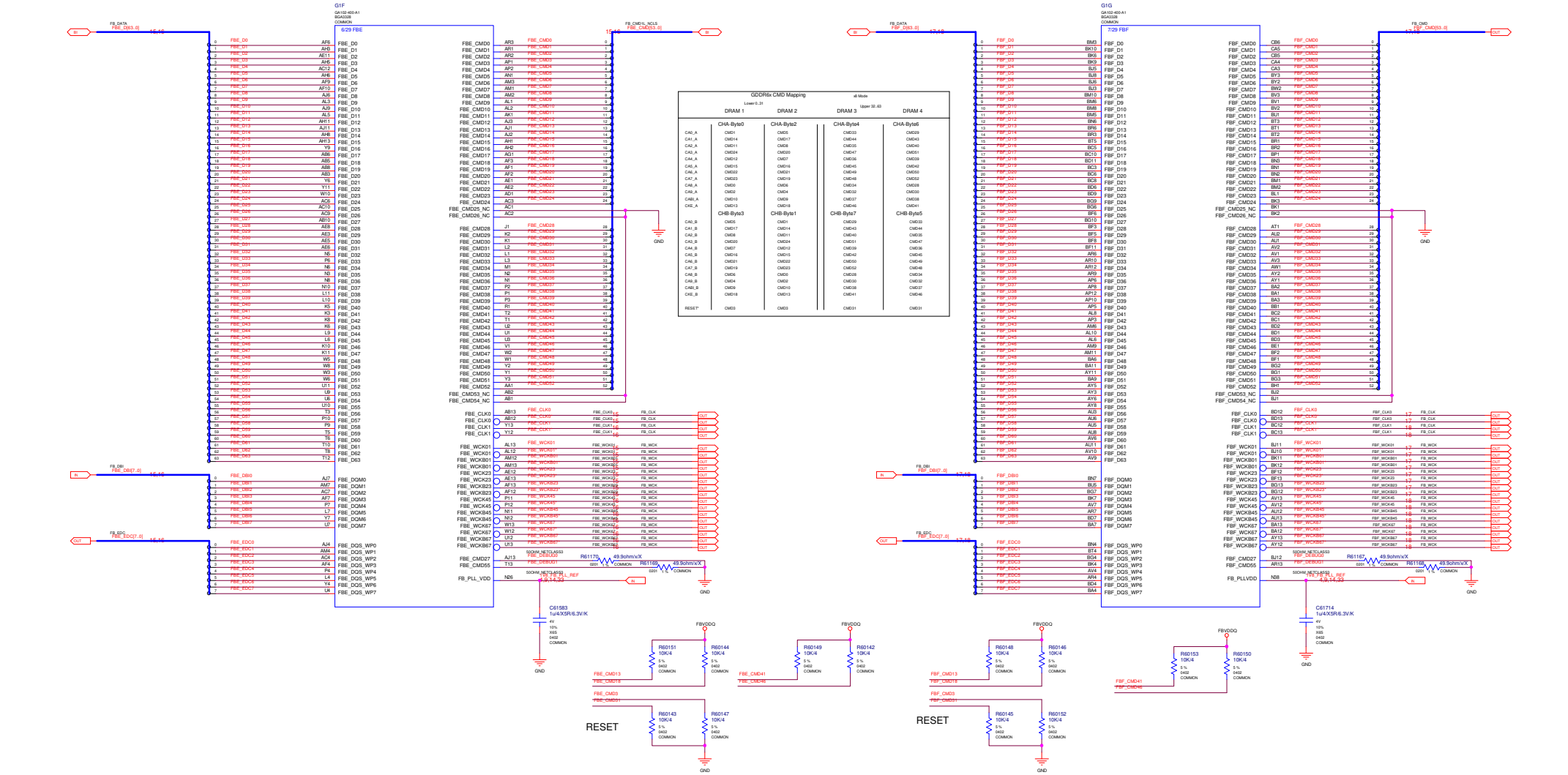
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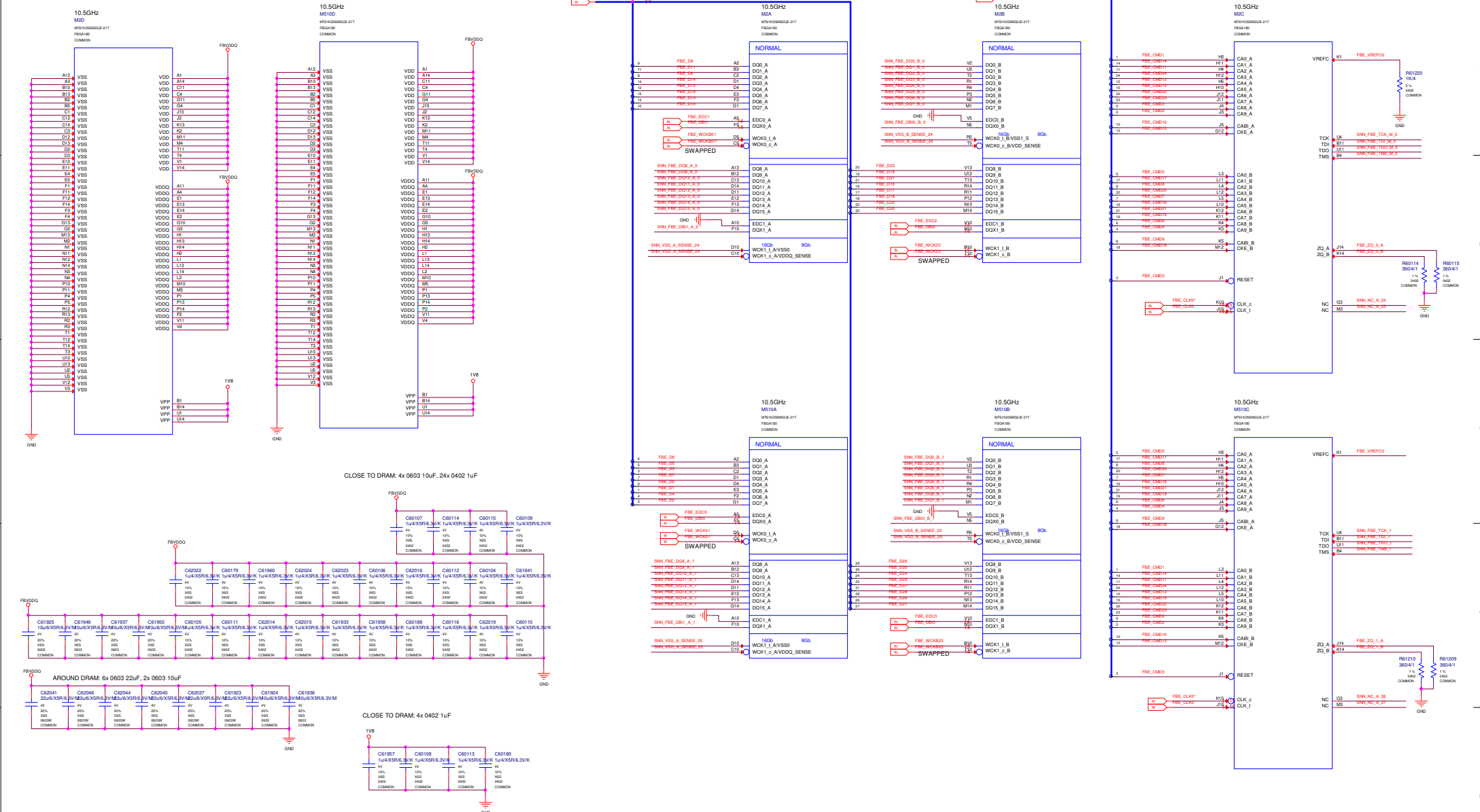


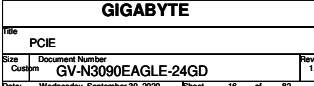
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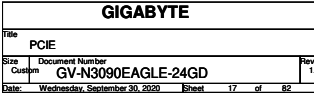


MEMORY: GPU Partition E/F

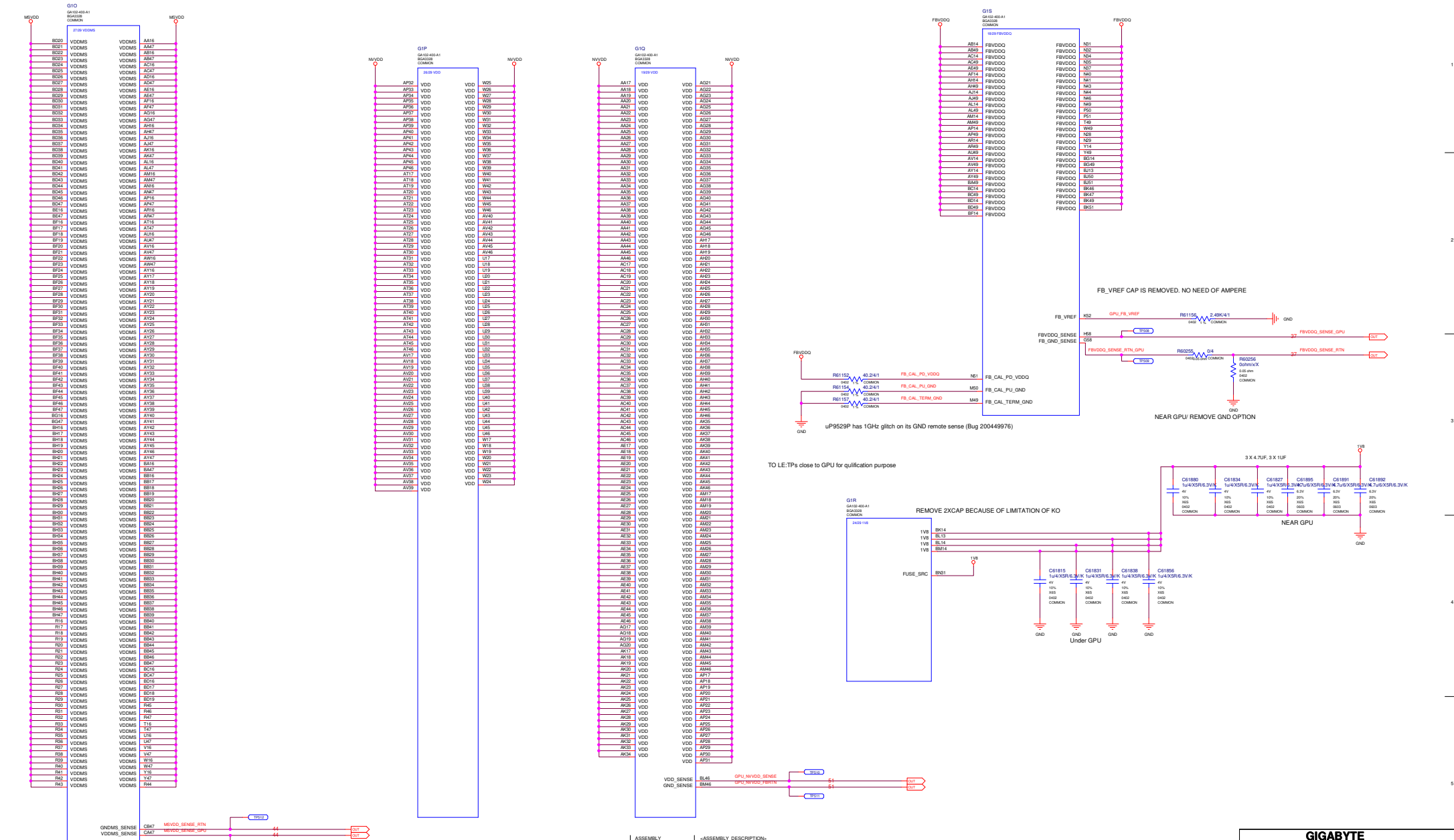








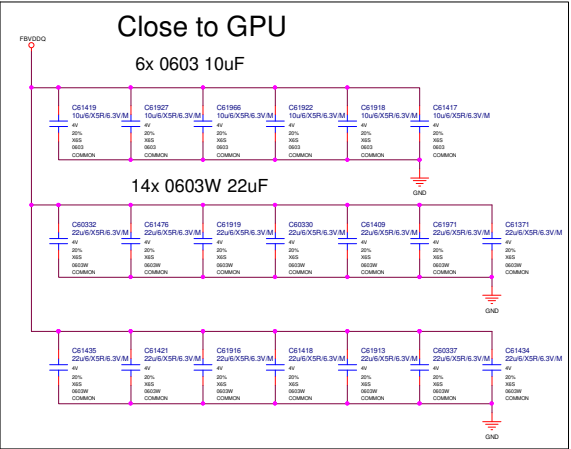
GPU PWR and GND



NVVDD UNDER GPU

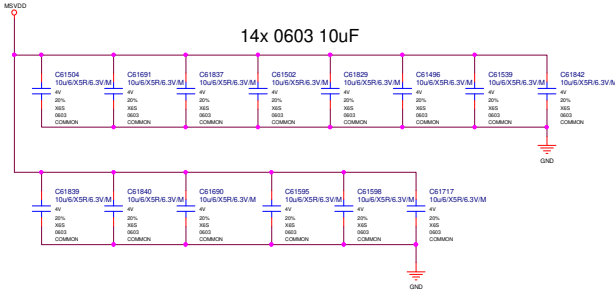


FBVDDQ

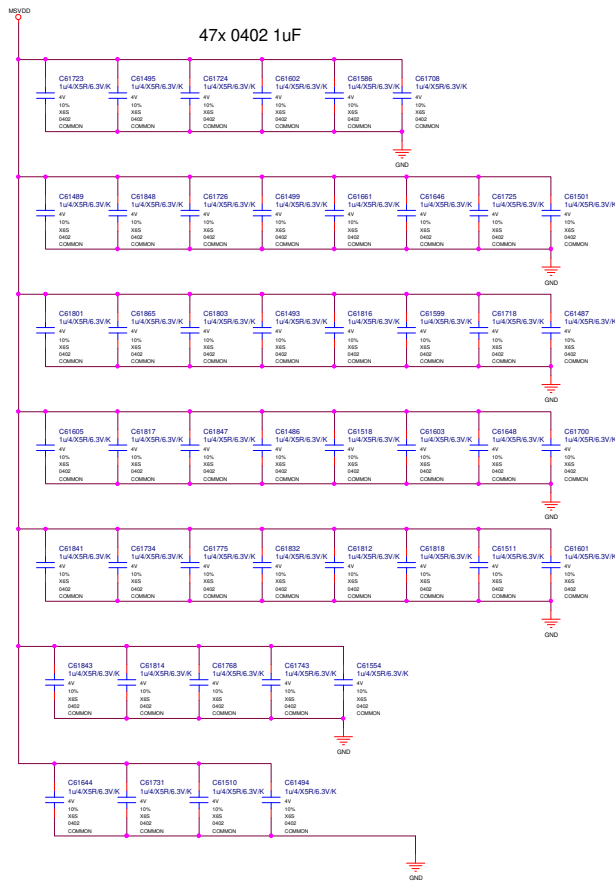
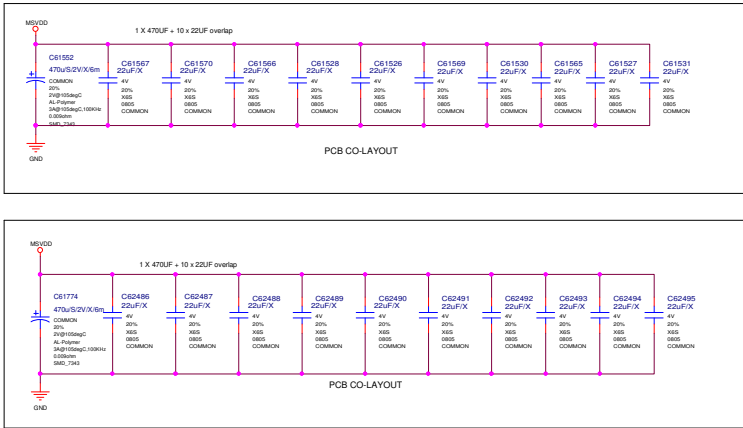


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

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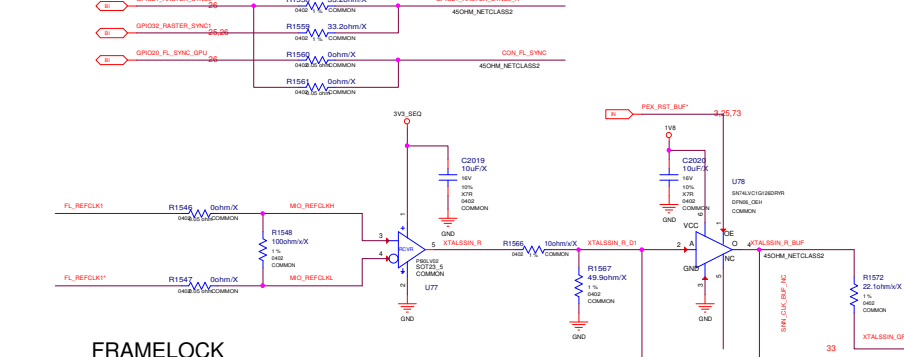
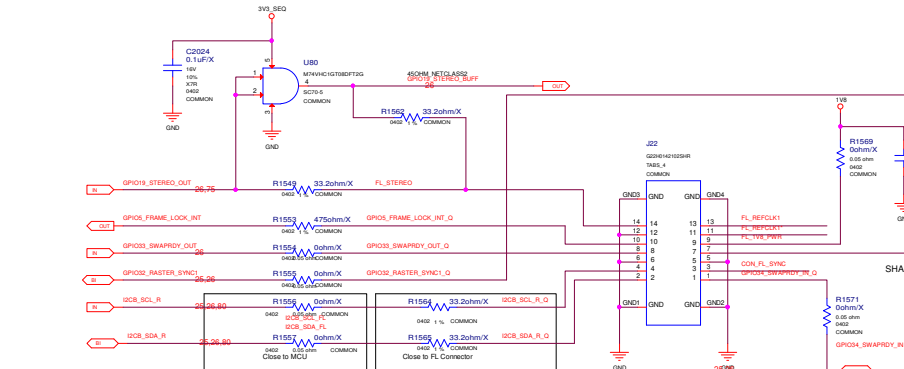
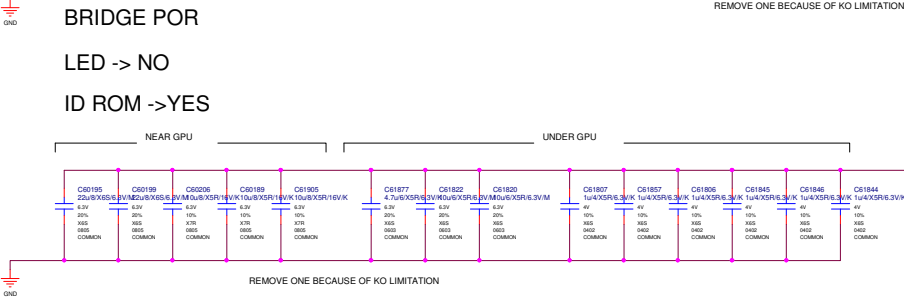
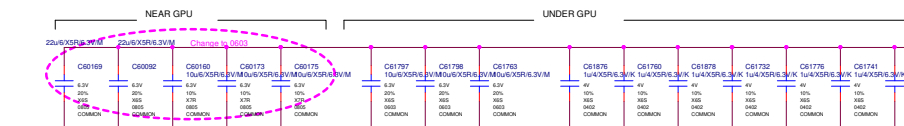
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| Title | | | |
| PCIE | | | |
| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | | Sheet 24 of 82 |

NVHS Interface and FRAME LOCK

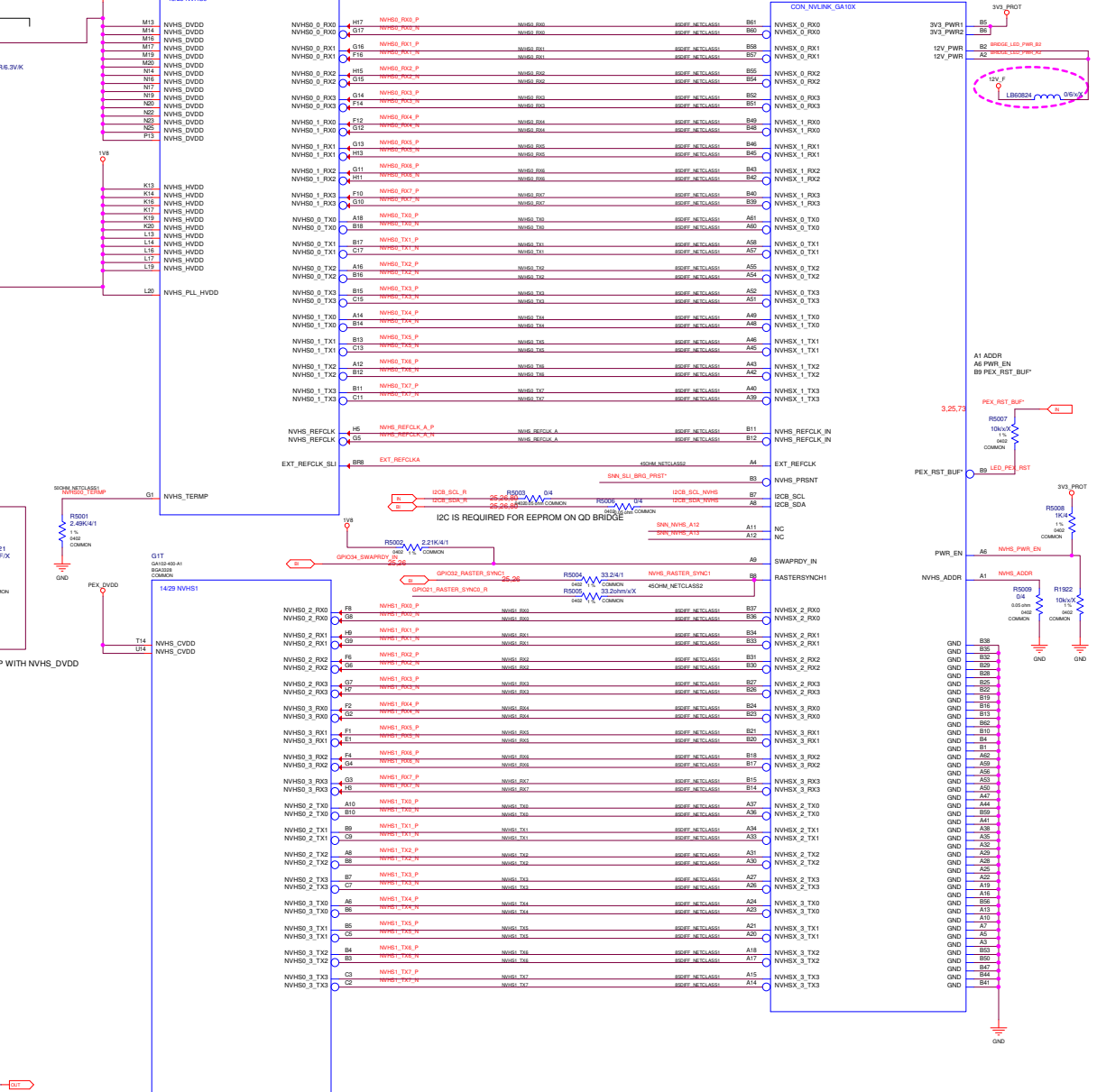


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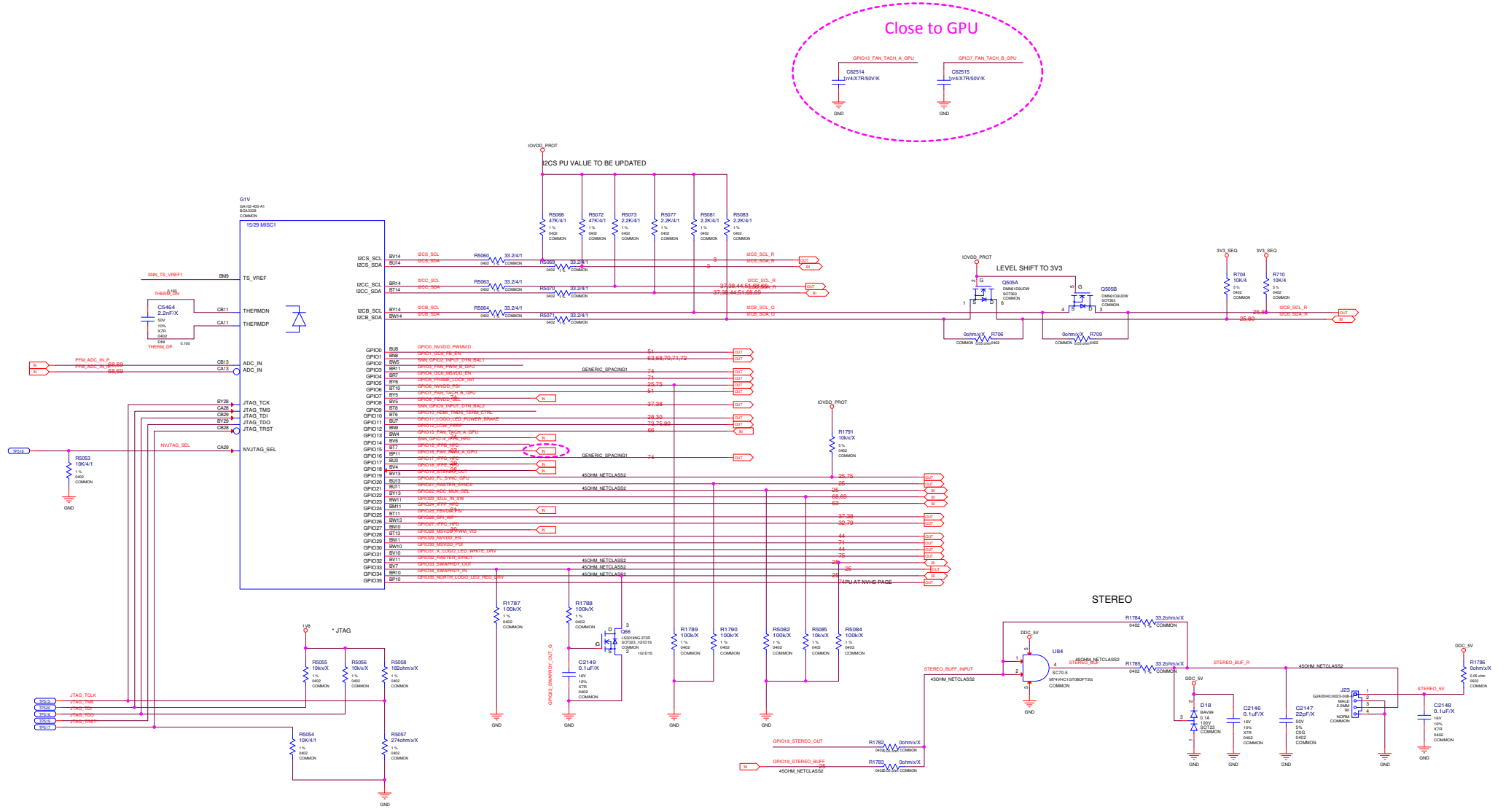
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NVHS v16

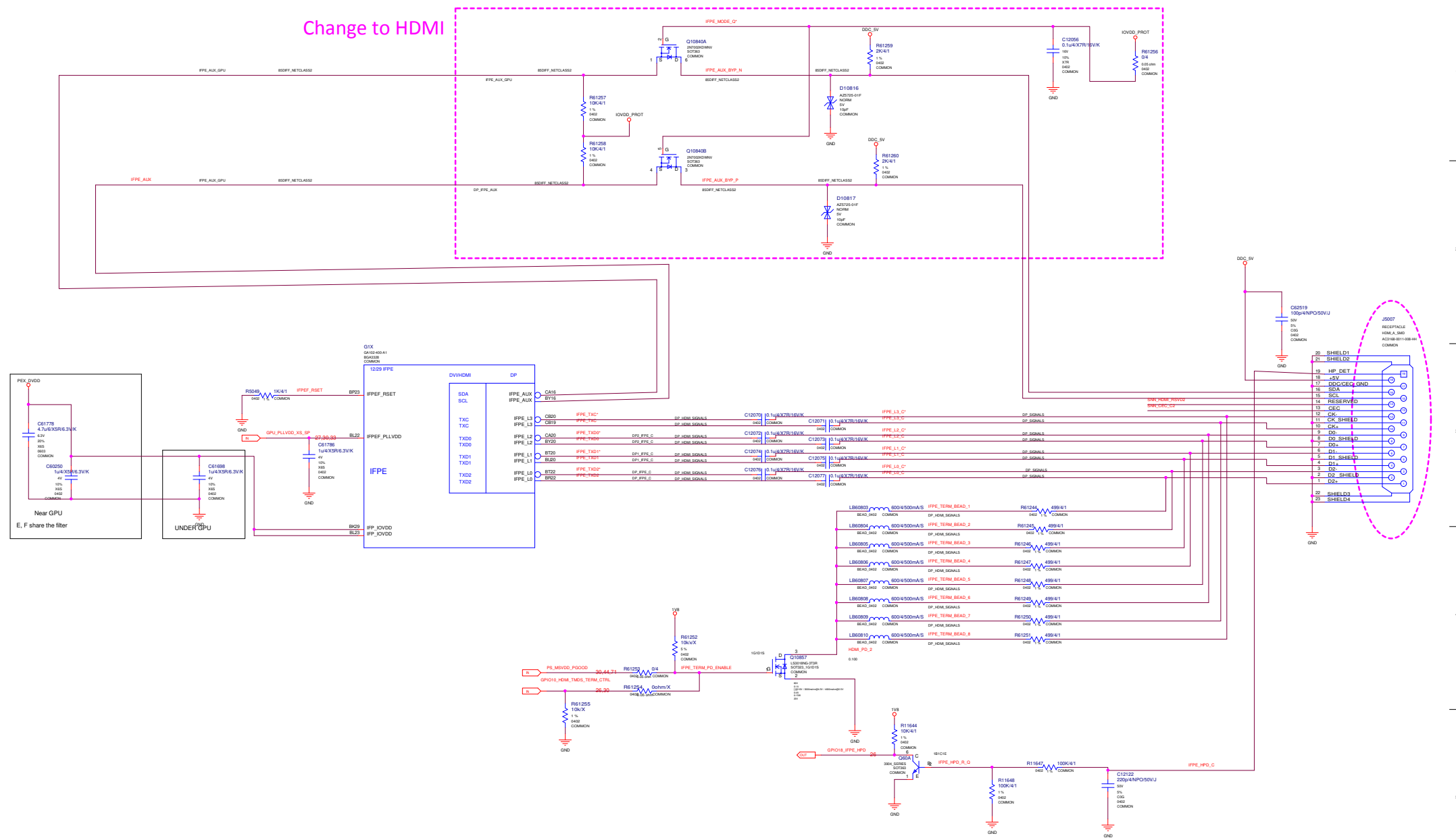


MISC1: Fan, Thermal, JTAG, GPIO, STEREO

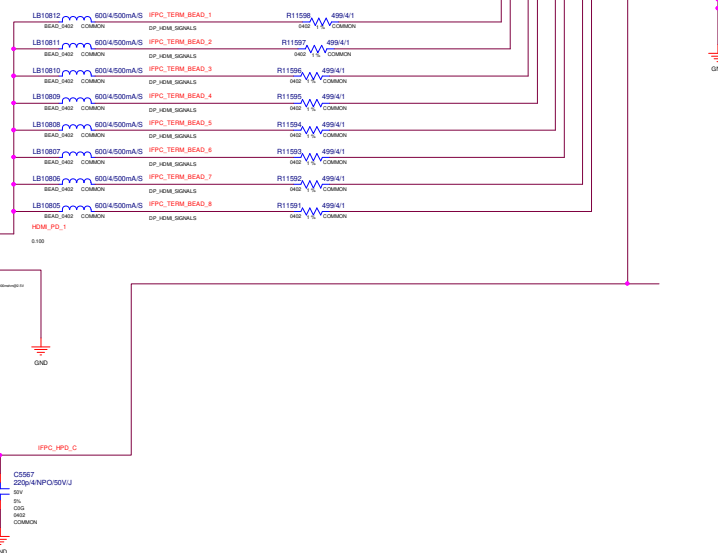
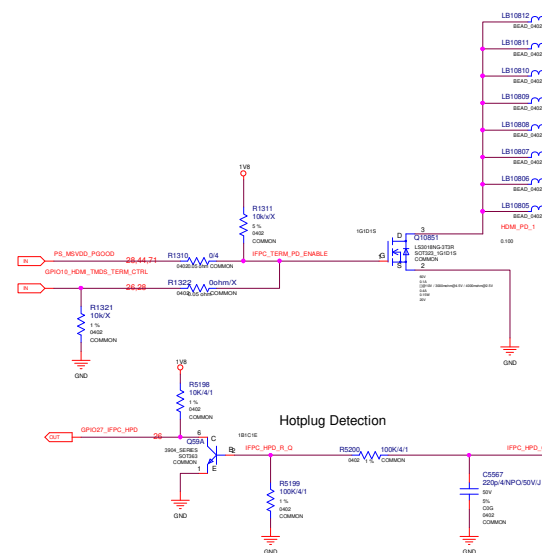
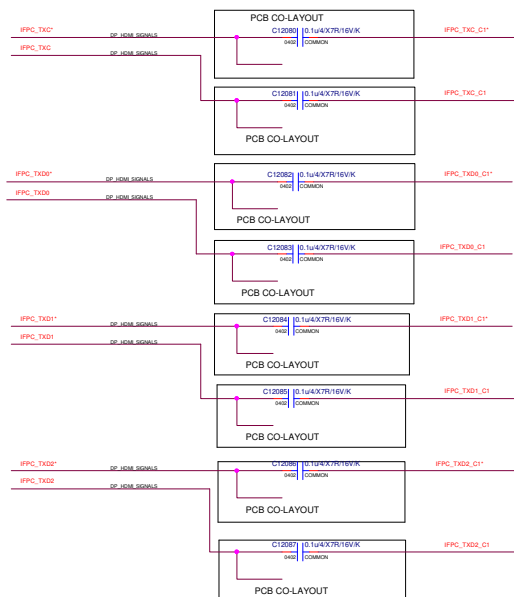
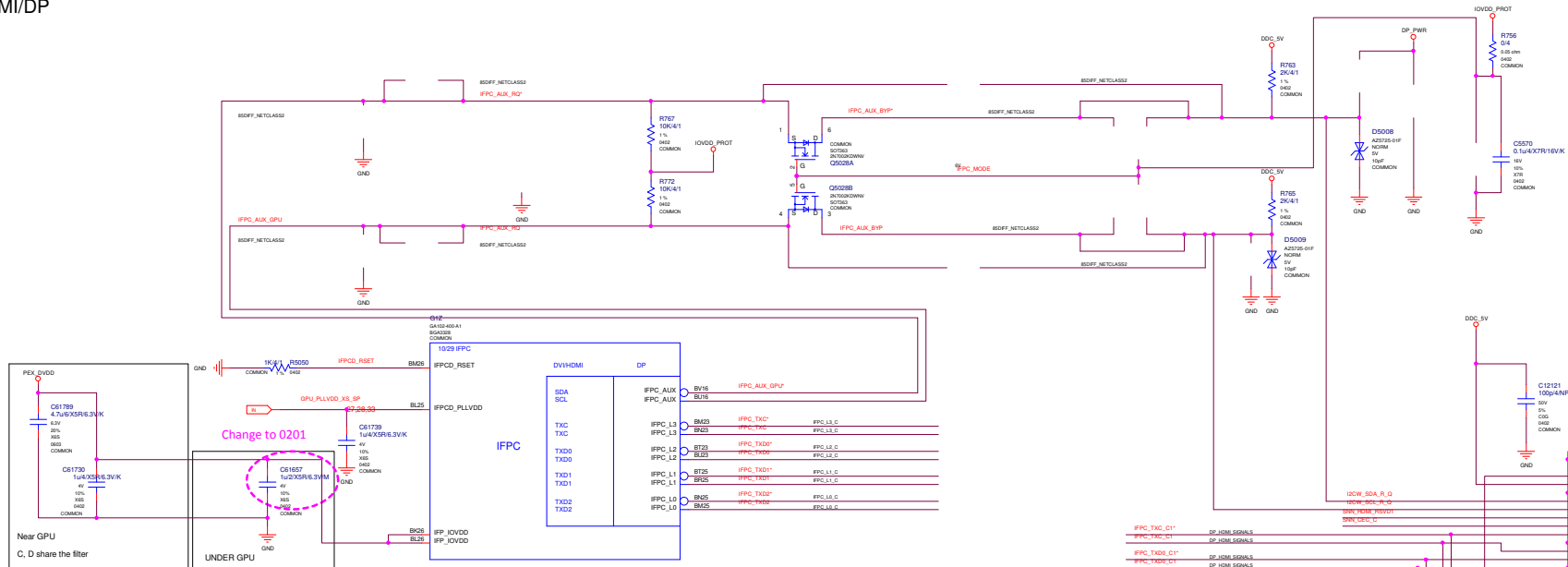


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Change to HDMI



IFPC HDMI/DP



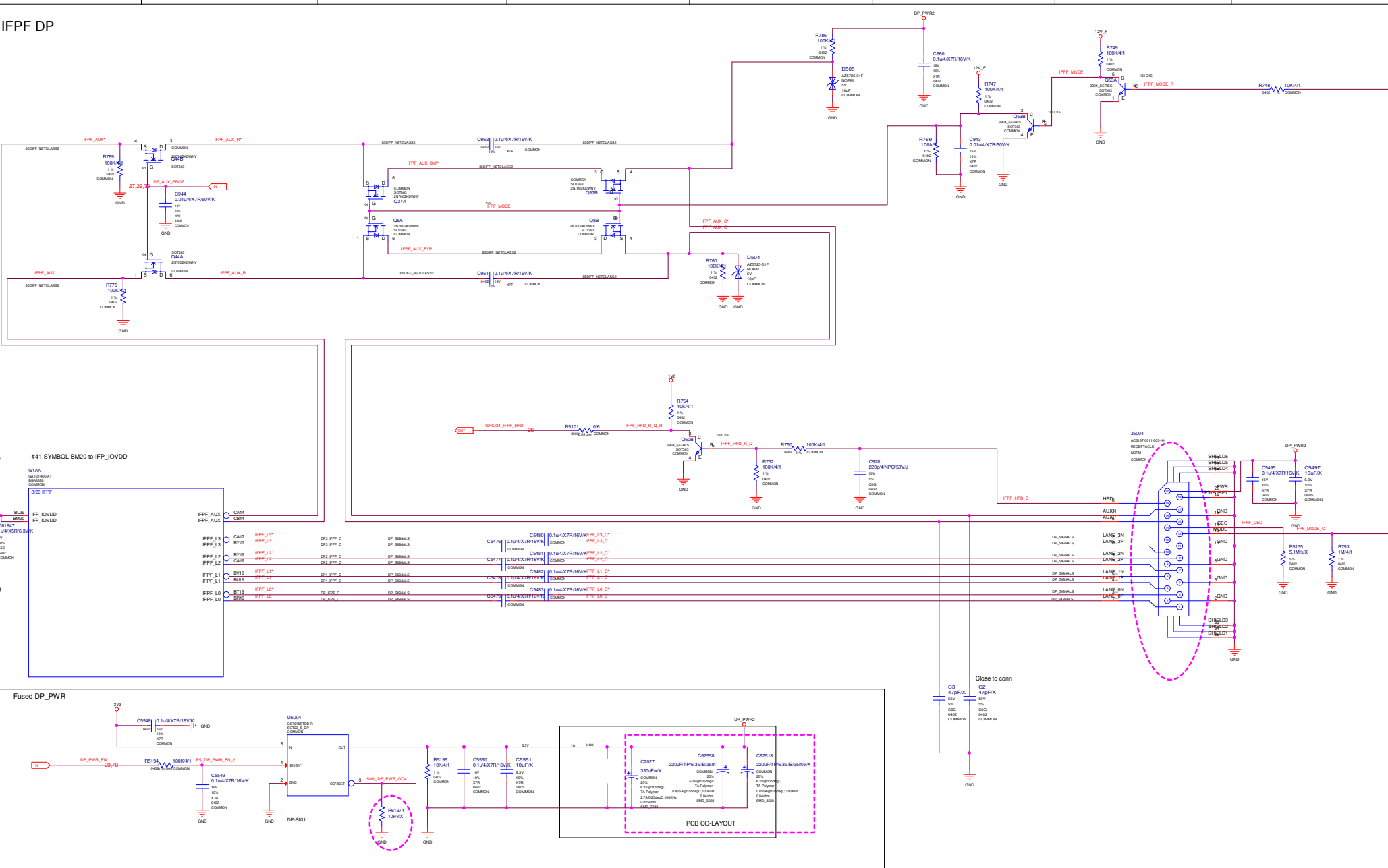
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GIGABYTE

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| Title | | | |
| PCIE | | | |
| Size | Document Number | Rev | |
| Custom | GV-N3090EAGLE-24GD | 1.0 | |
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IFPF DP



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MISC: ROM, Straps

| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] | |
|--------|--------|--------|-------------|--------------------------|
| L | L | L | 00000 | RAMCFG MICRON 8Gb 19Gbps |
| L | H | L | 00010 | RAMCFG TBD |
| H | L | L | 00100 | RAMCFG TBD |
| H | L | H | 00101 | RAMCFG TBD |
| H | L | H | 00101 | RAMCFG MICRON 8Gb 21Gbps |

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

DEFAULT

| ROM_SO | ROM_SI | ROM_SCLK | SMARTFAN[2:0].FS_OVERT | 1:ENABLE 0:DISABLE |
|--------|--------|----------|------------------------|--------------------|
| H | H | H | 0111 | FS_OVERT ENABLE |
| L | L | L | 0000 | FS_OVERT DISABLE |

DEFAULT

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|--------|--------|--------|--------------|-----------|----------|------------|
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | H | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 |
| L | L | L | 0 | 0 | 0 | 0 |

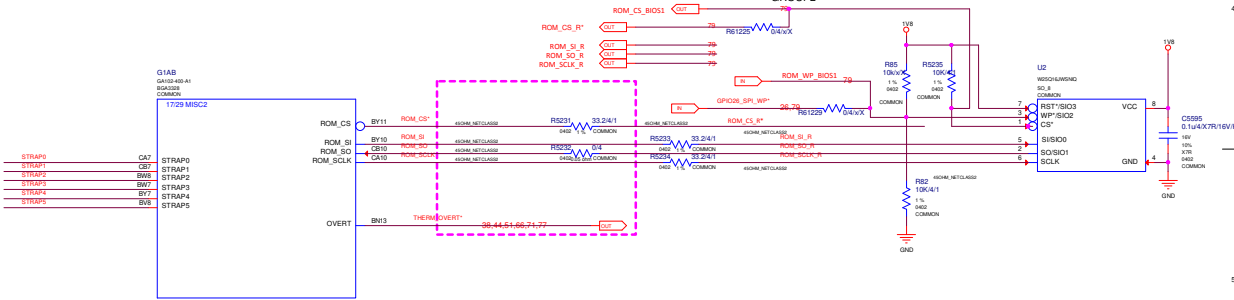
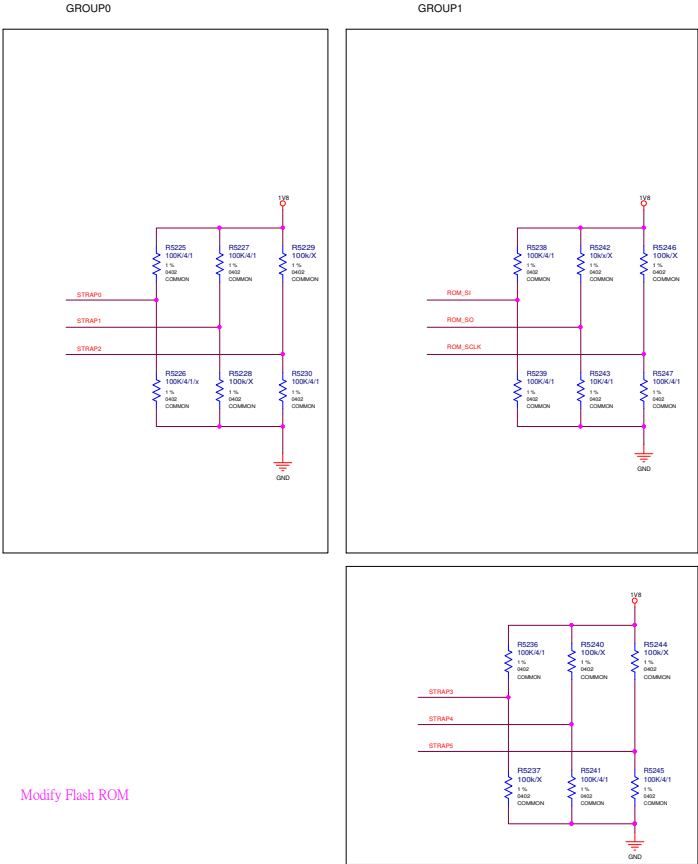
Default

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

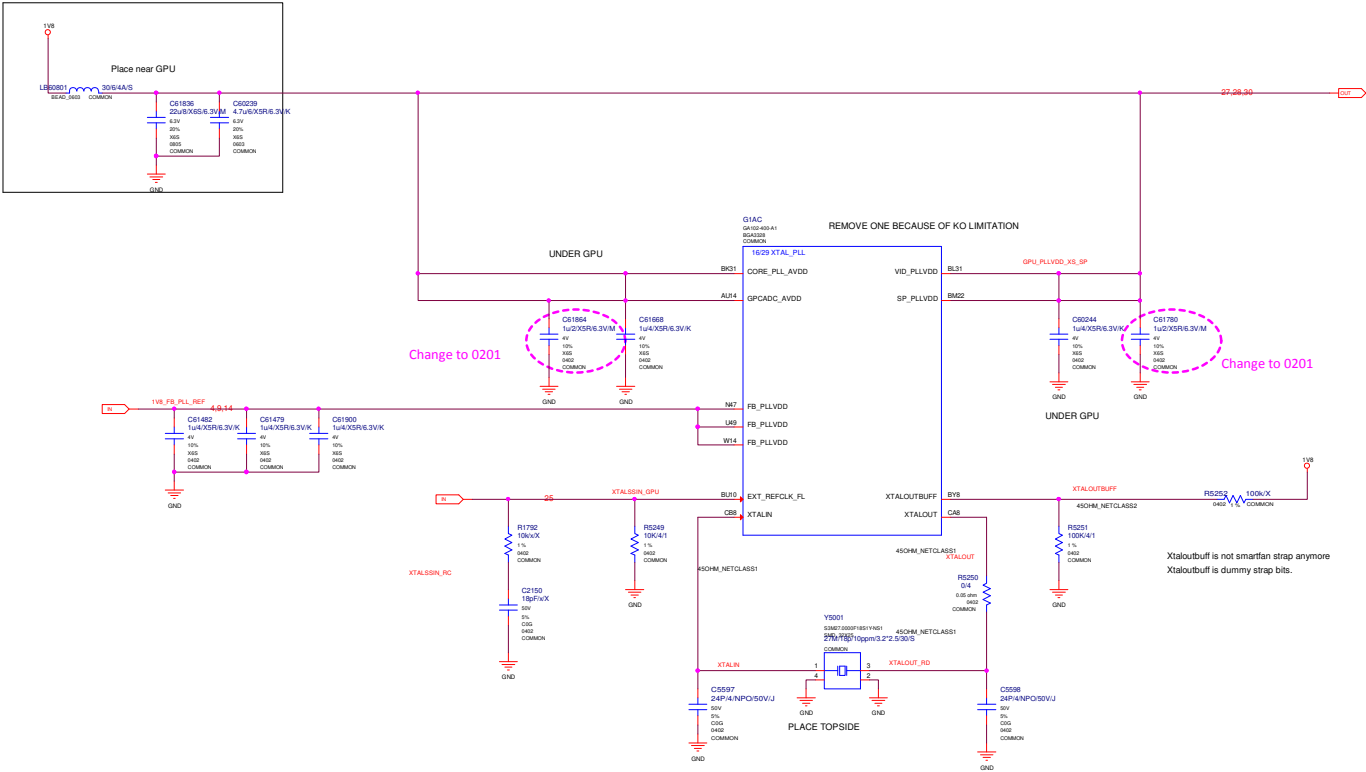
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

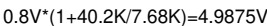
1:VGA_DEVICE ENABLE
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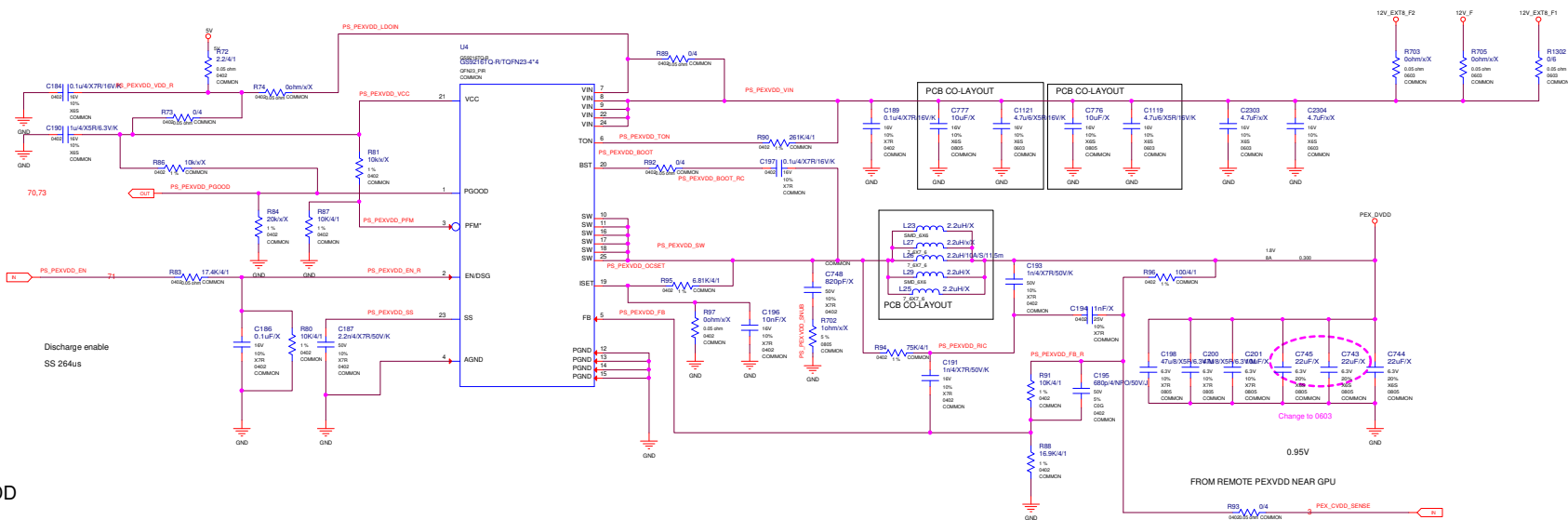
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MISC: XTAL. PLL

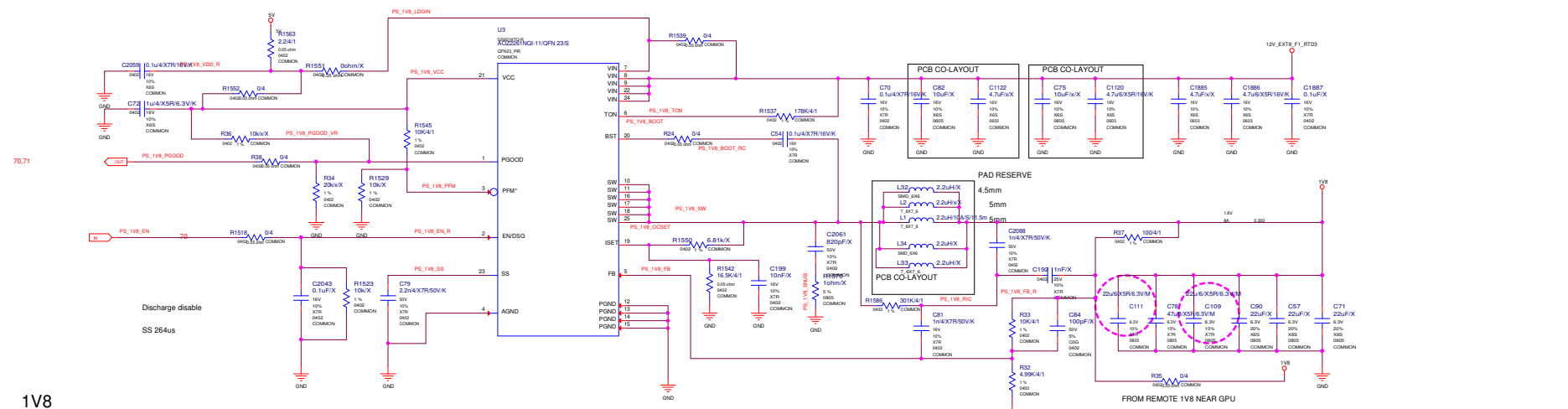




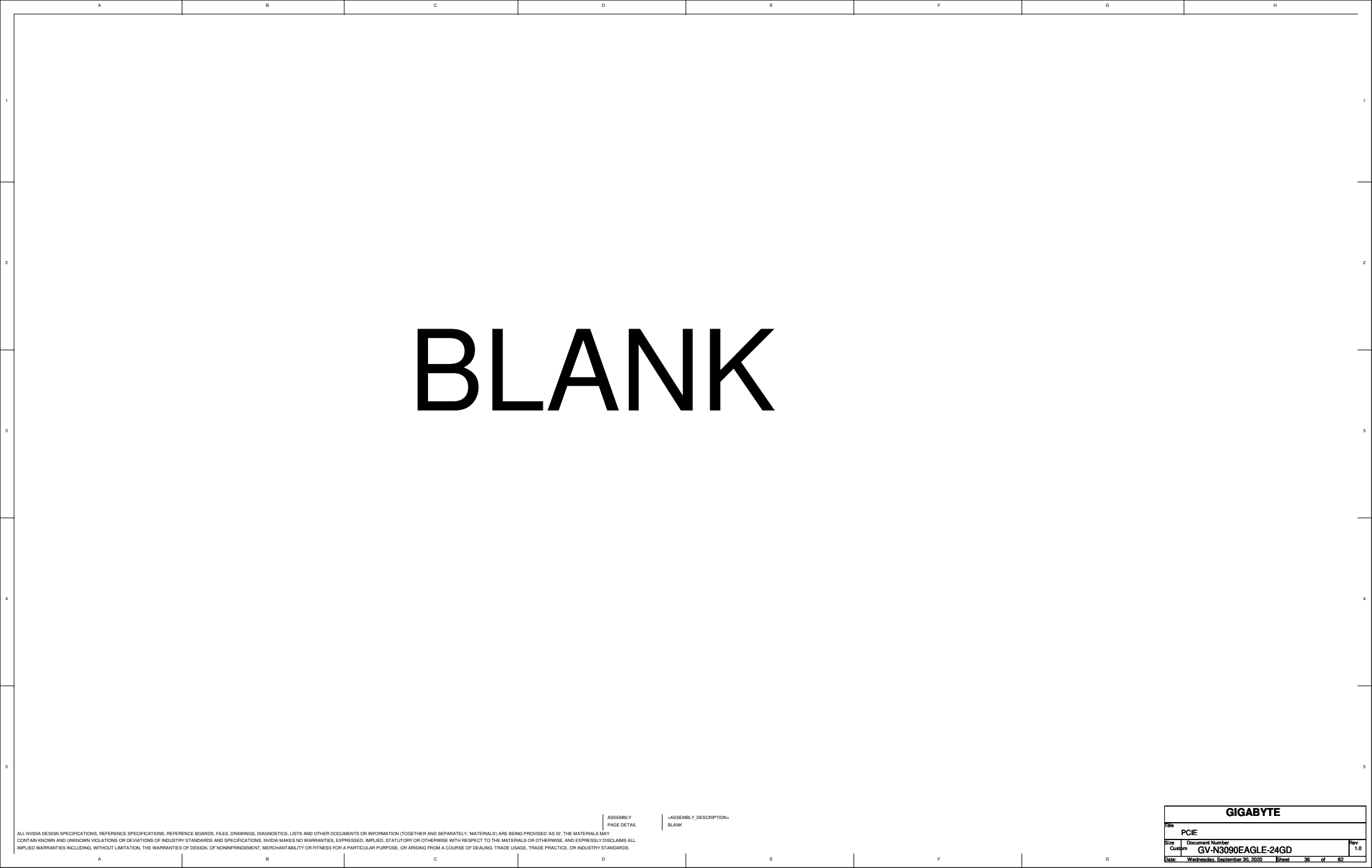
PS: PEX DVDD 1V8 Rail



PEX DVDD



1V8



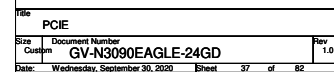
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ASSEMBLY
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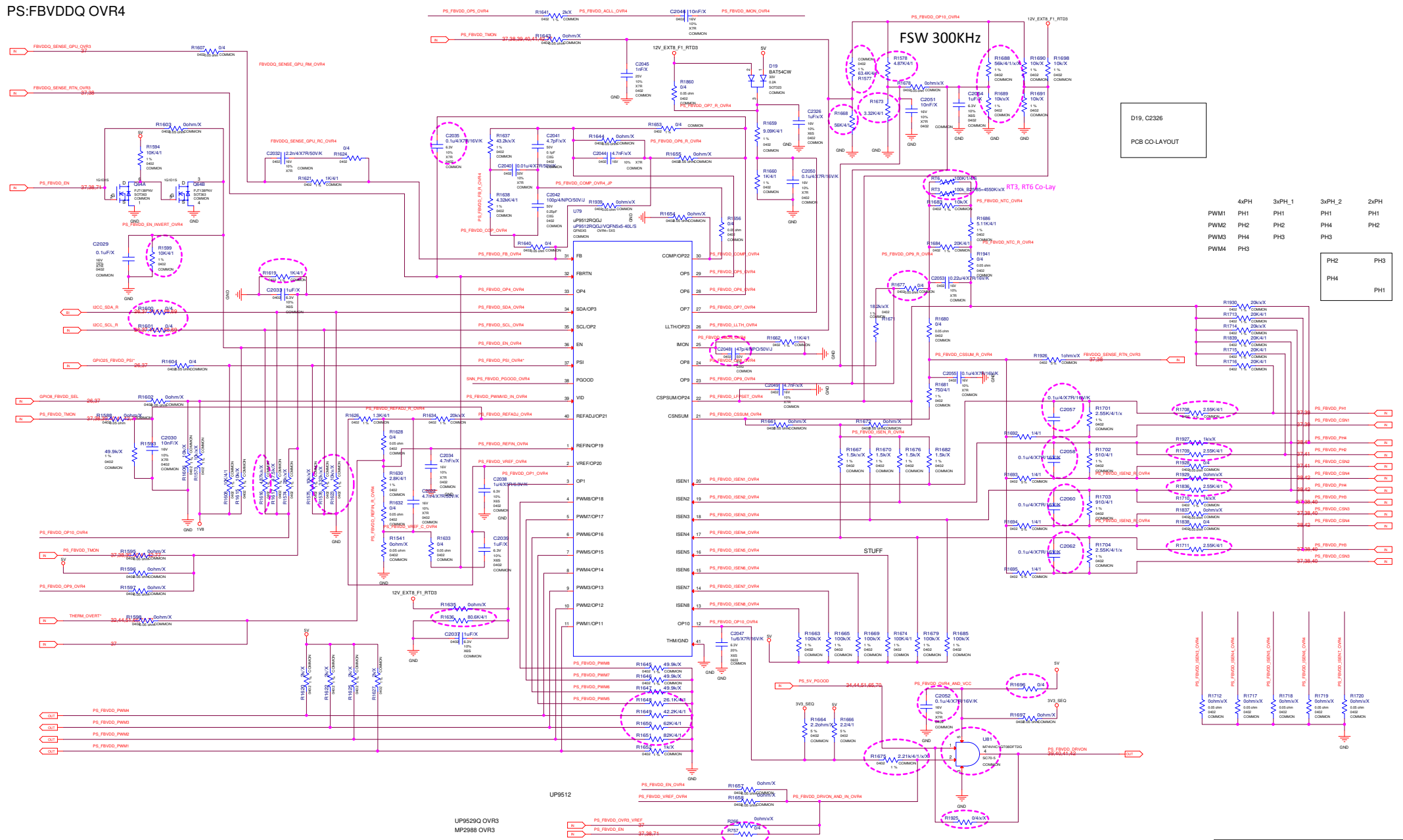
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| Size | Document Number | | Rev |
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| Date: | Wednesday, September 30, 2020 | | Sheet 36 of 82 |

FOR DT SKU

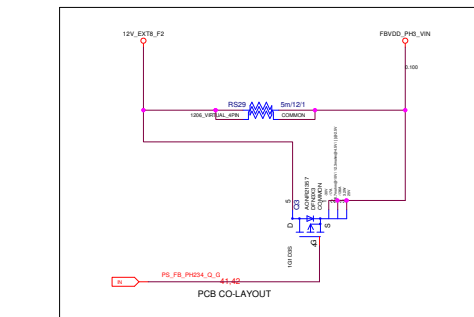
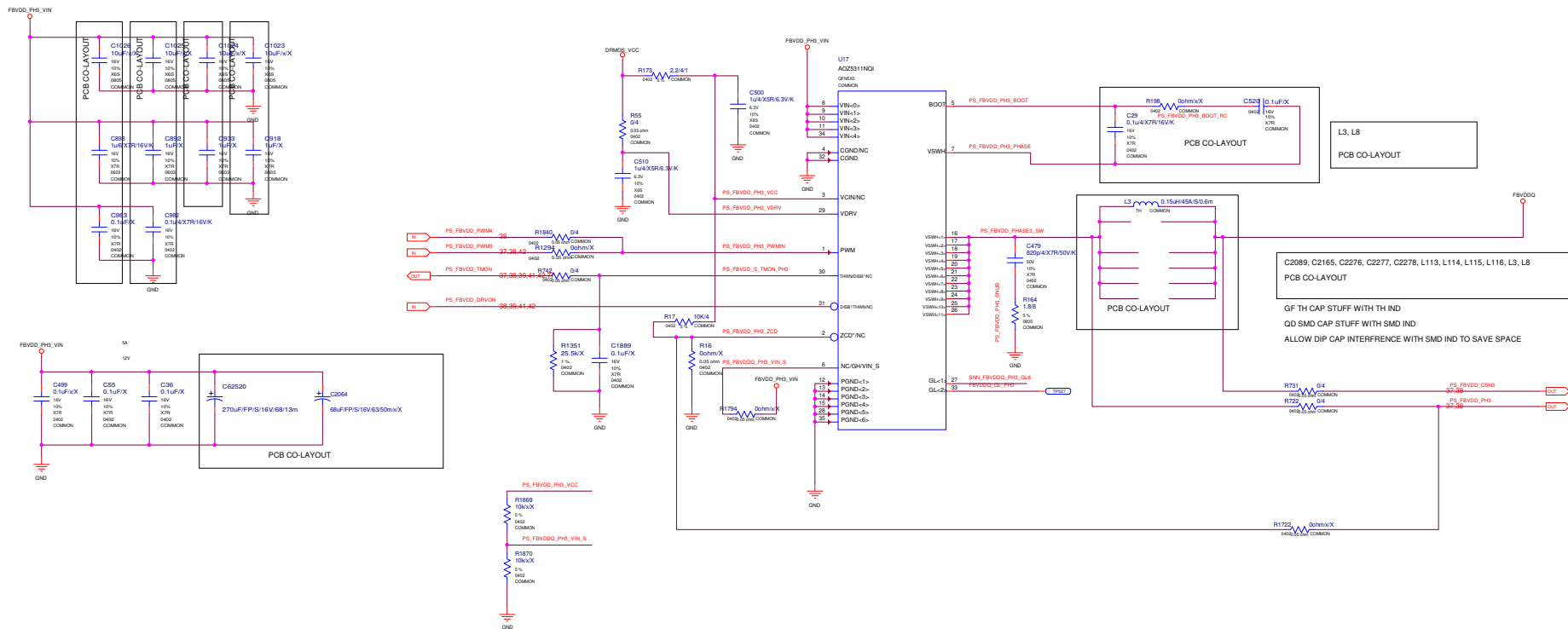


PS:FBVDDQ OVR4



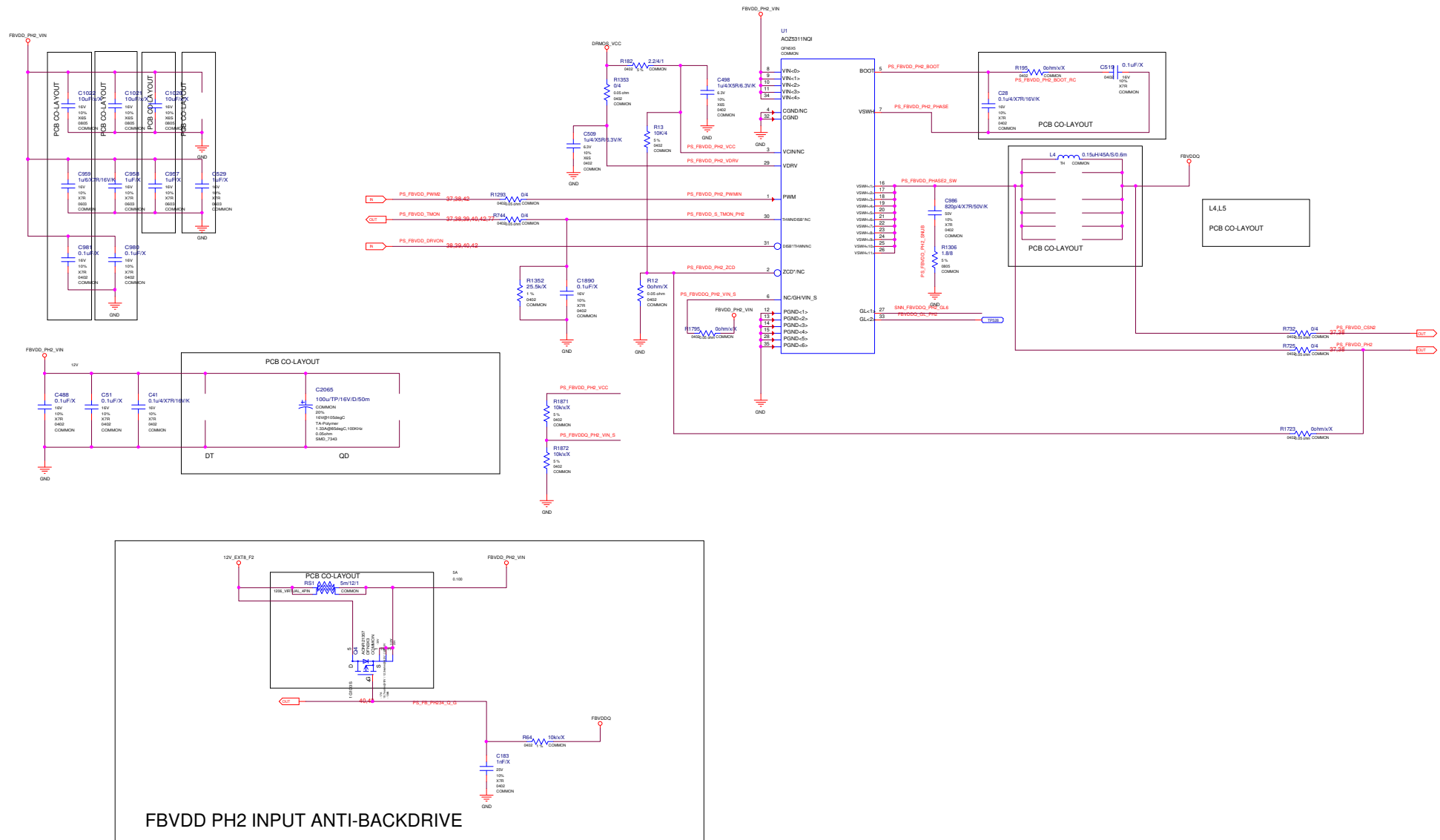
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PS: FBVDD PH3

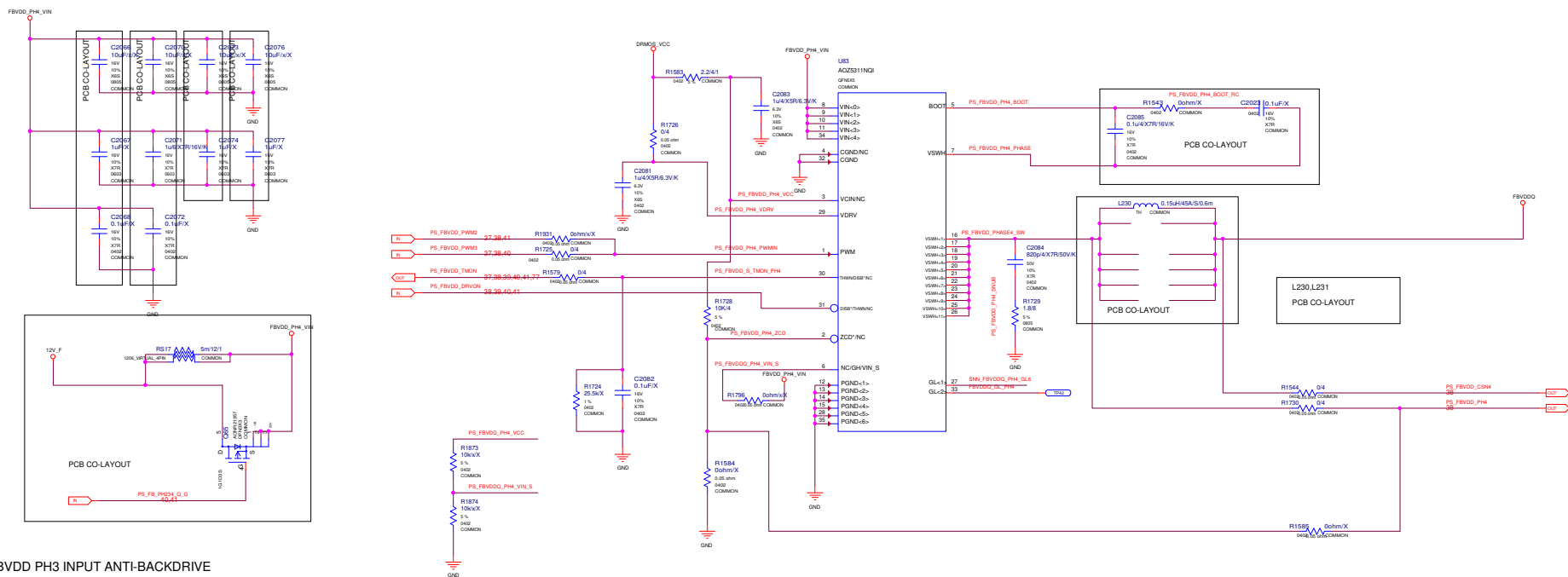


FBVDD PH3 INPUT ANTI-BACKDRIVE

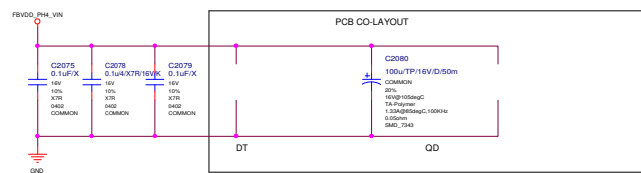
PS: FBVDD PH2



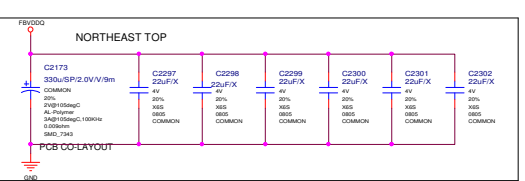
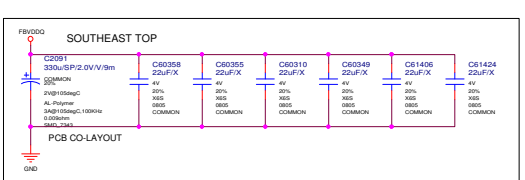
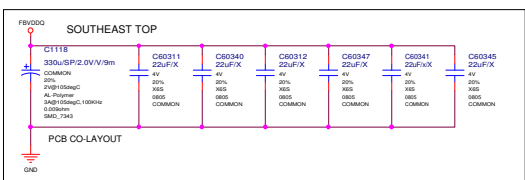
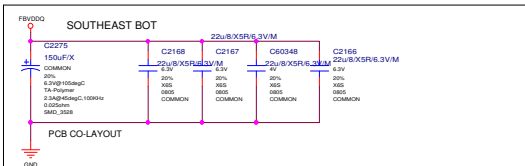
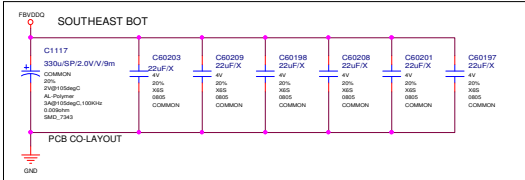
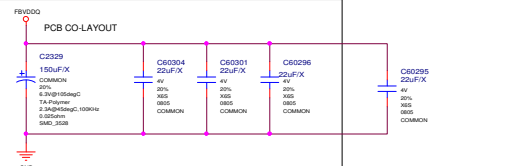
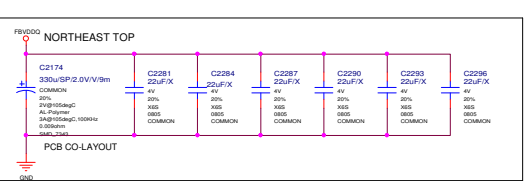
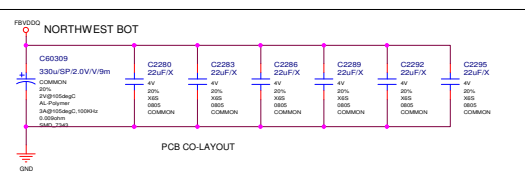
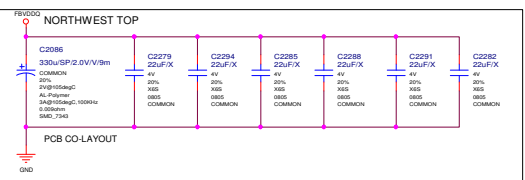
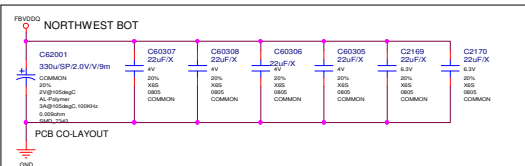
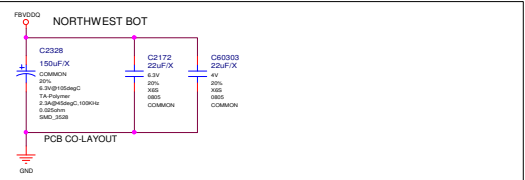
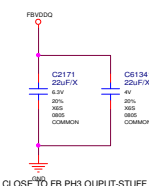
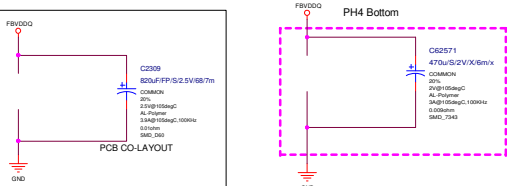
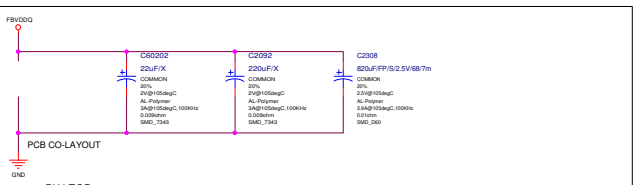
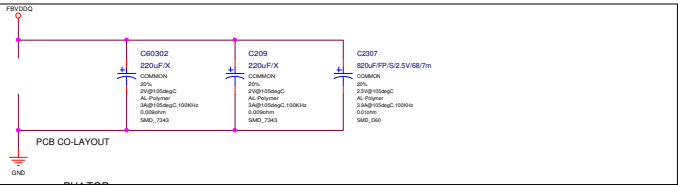
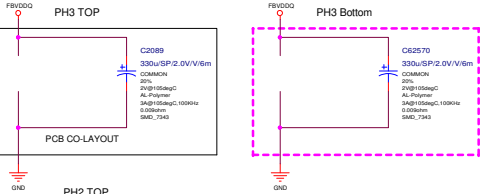
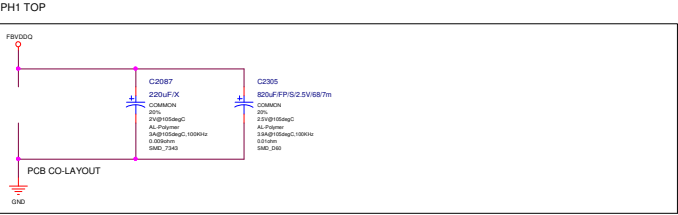
PS: FBVDD PH4



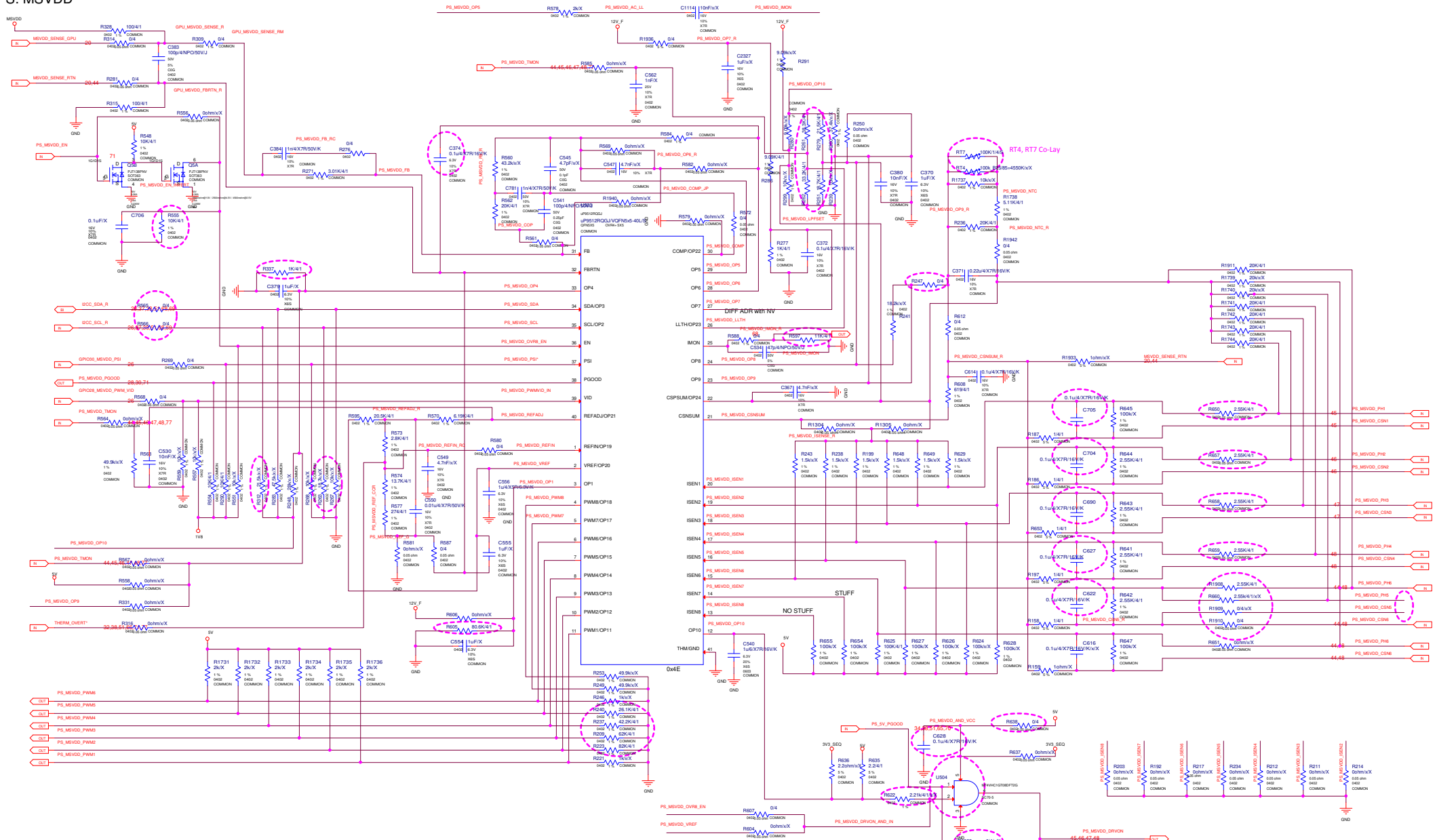
FBVDD PH3 INPUT ANTI-BACKDRIVE



REFER TO PCB FOR BOM STUFFING



PS: MSVDD



ASSEMBLY
PAGE DETAIL

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PS: MSVDD CONTROLLER
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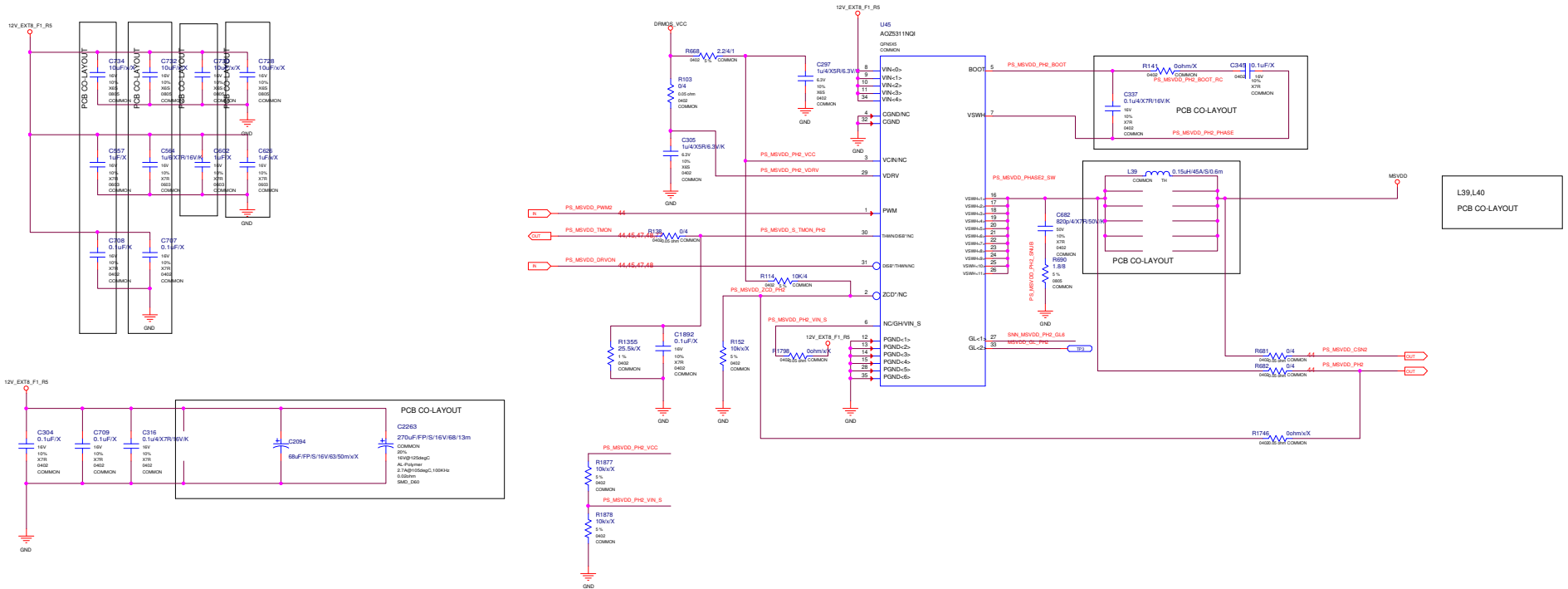
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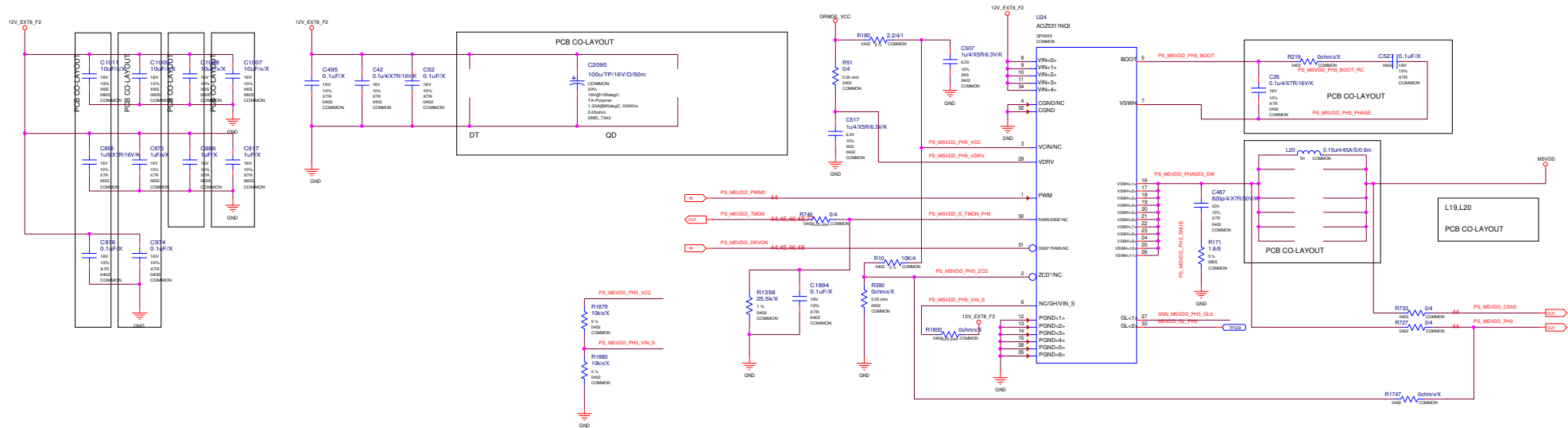
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| Size | Document Number |
| Custom | GV-N3090EAGLE-24GD |

Rev
1

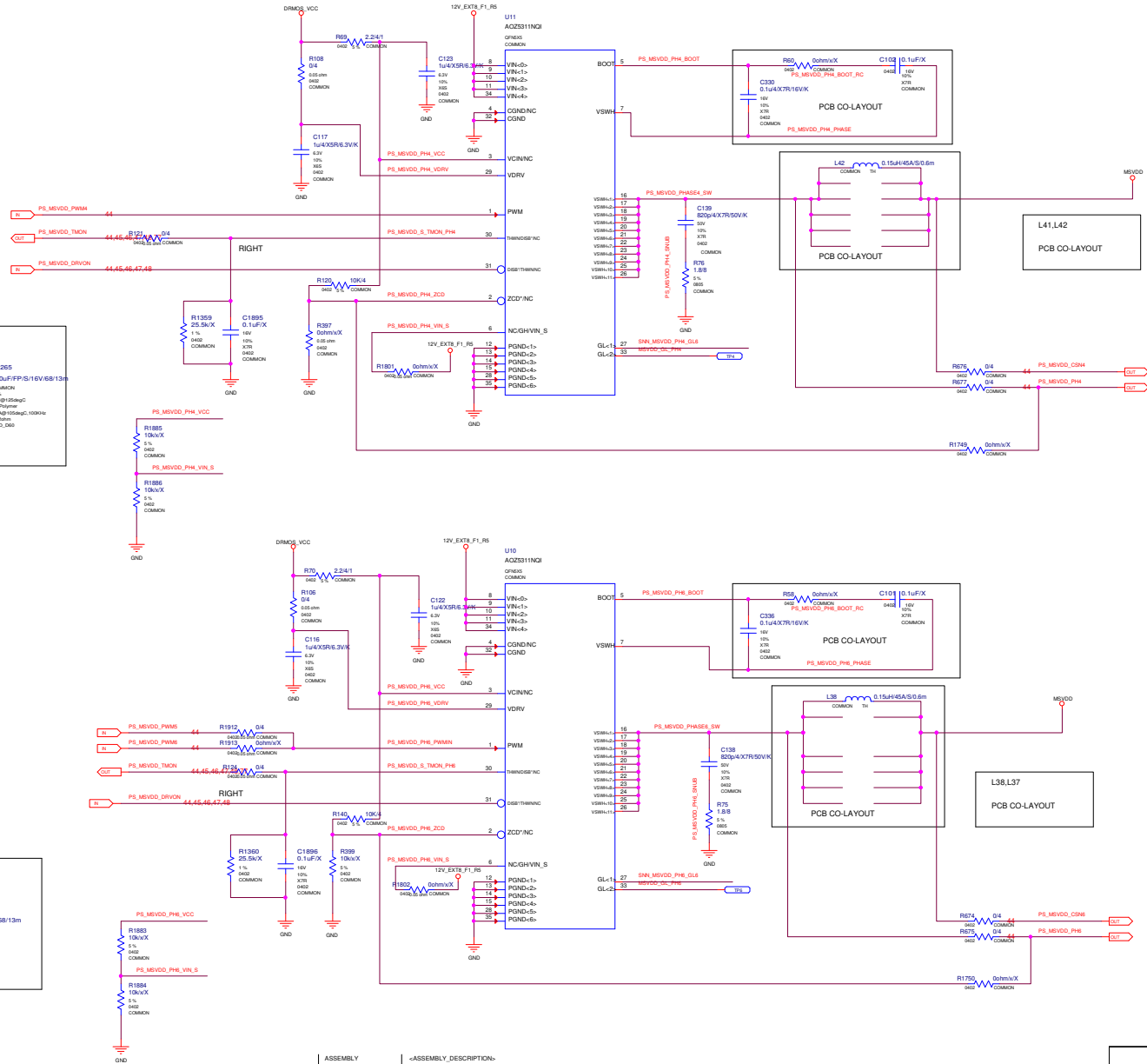
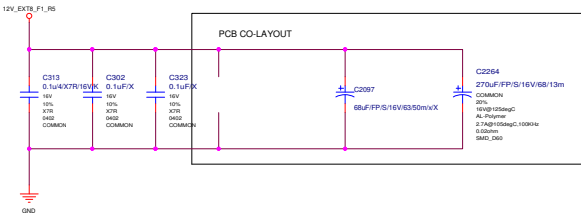
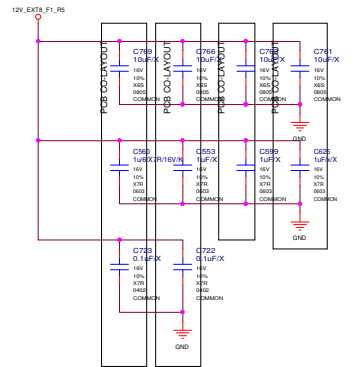
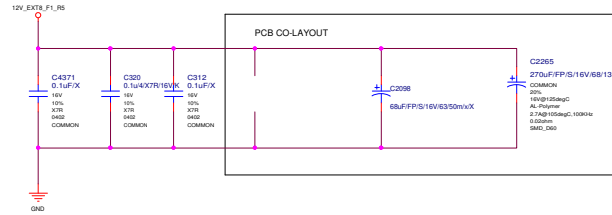
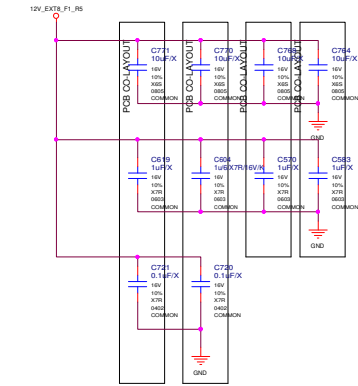
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PS:MSVDD Phase 3, 5

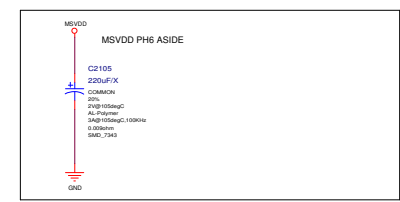
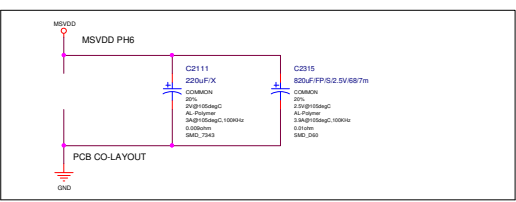
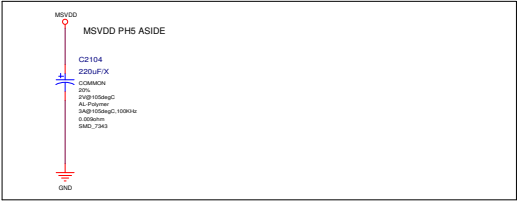
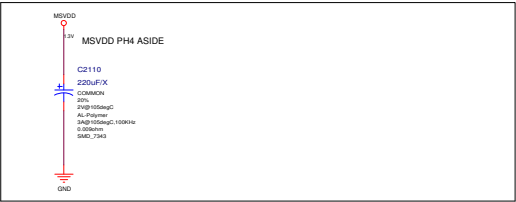
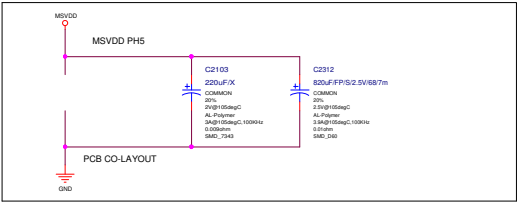
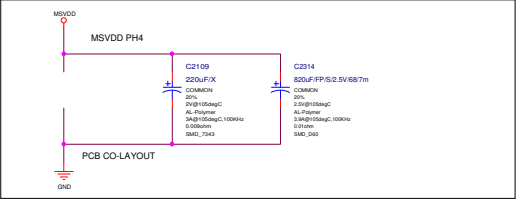
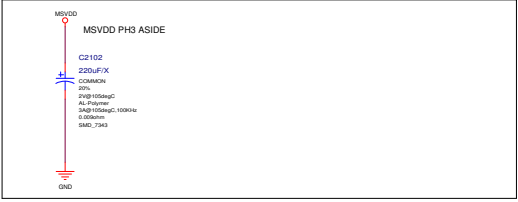
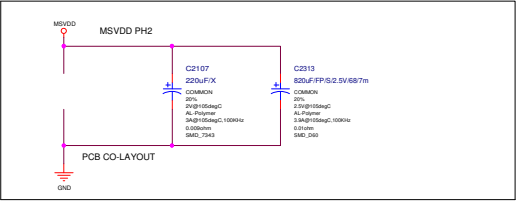
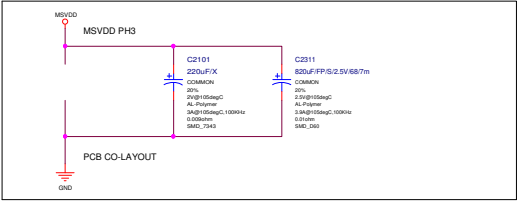
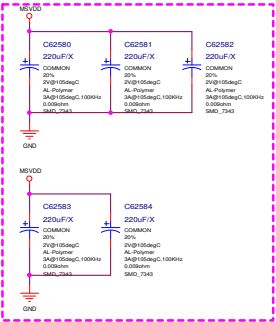
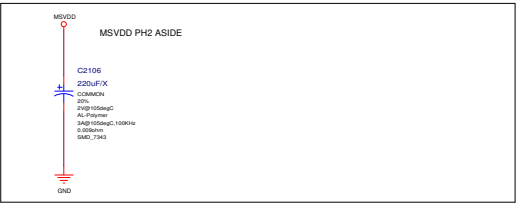
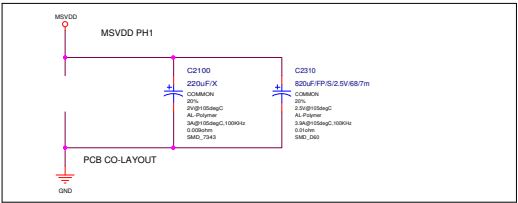


PS: MSVDD PH 4,6



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REFER TO PCB FOR BOM STUFFING



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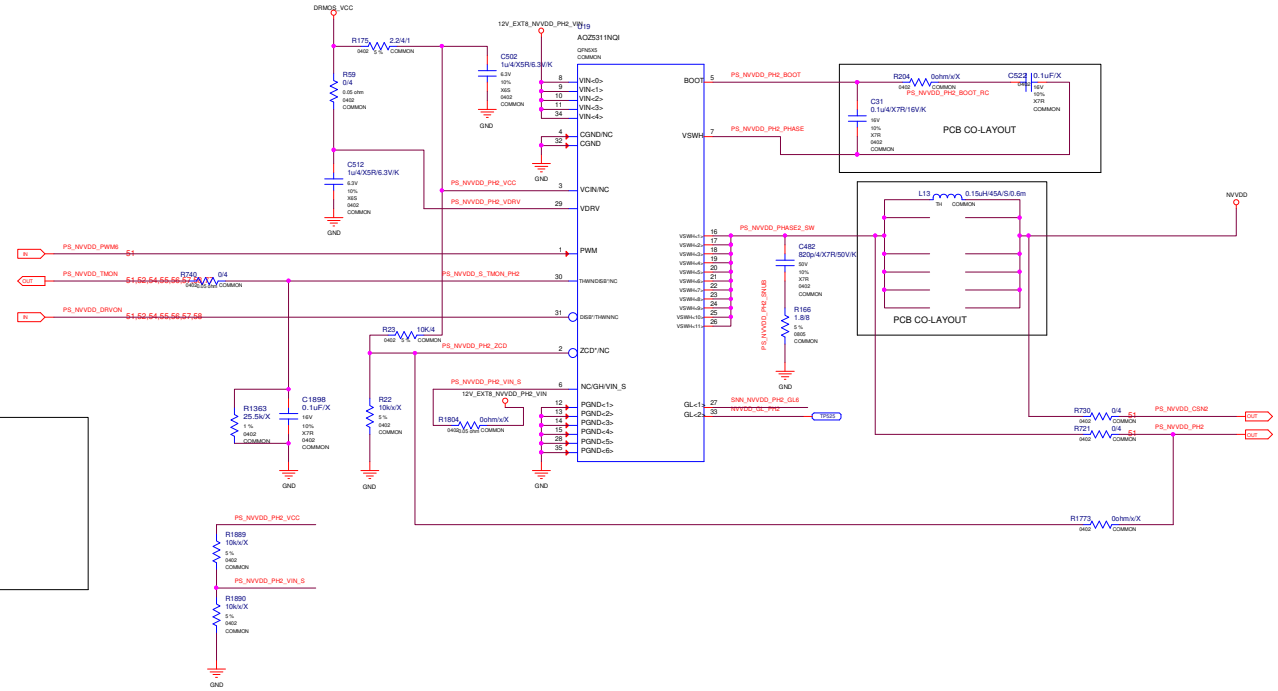
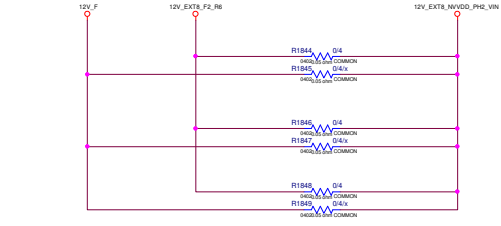
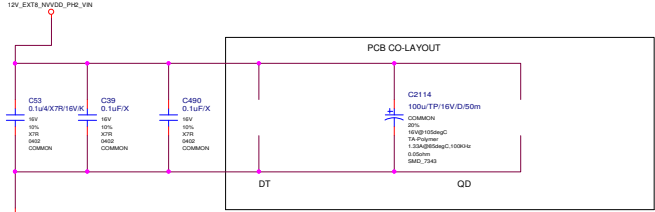
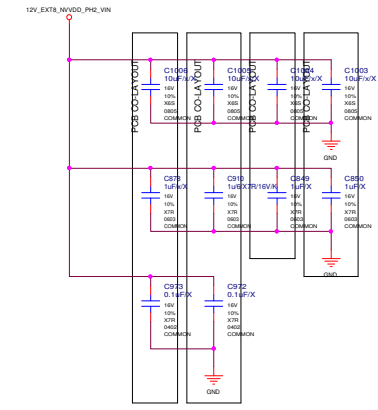
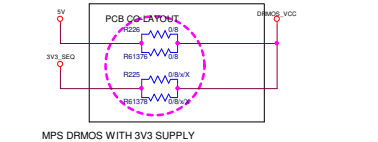
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| Title | | | |
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| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | Sheet | 50 of 82 |

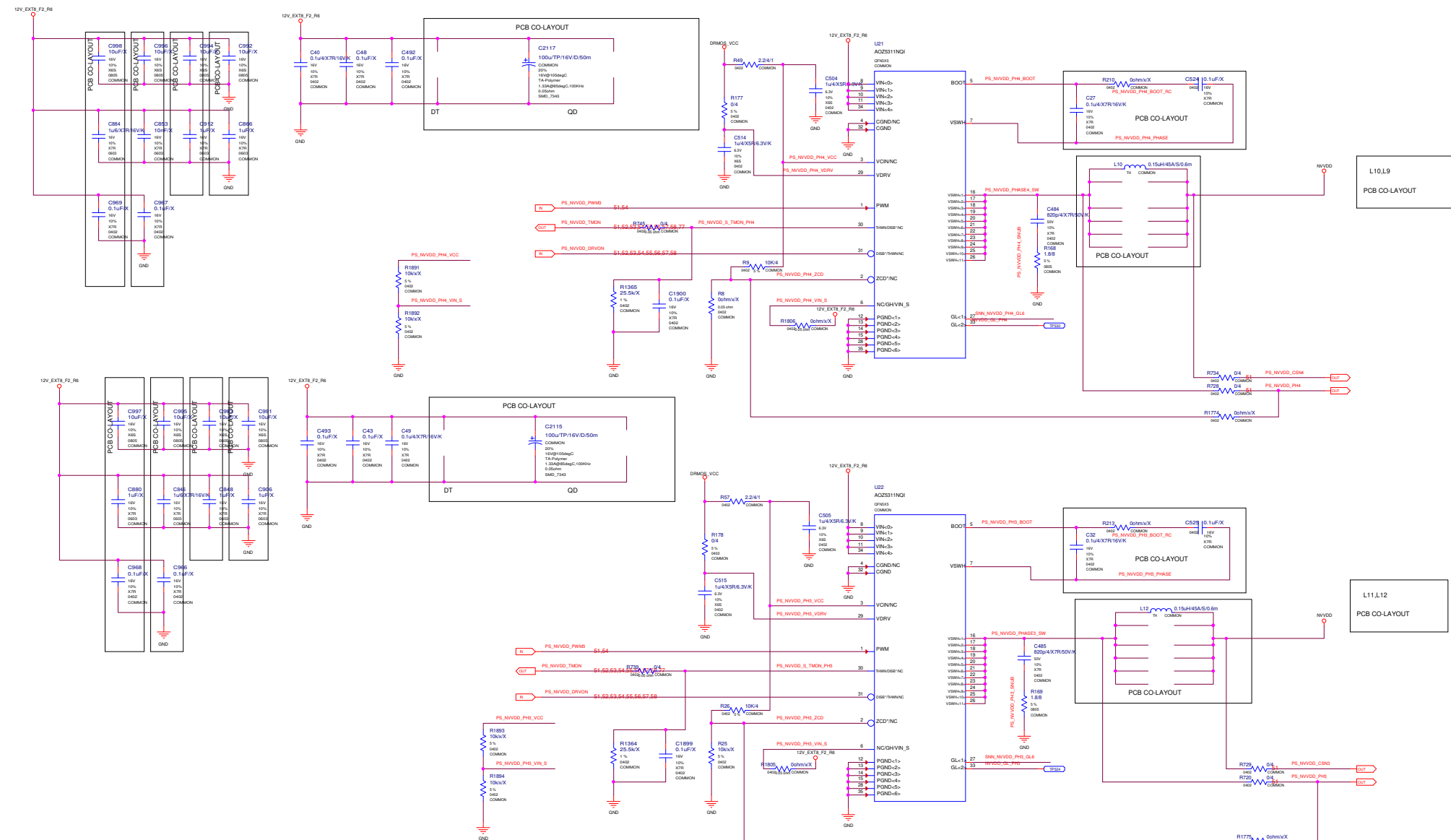
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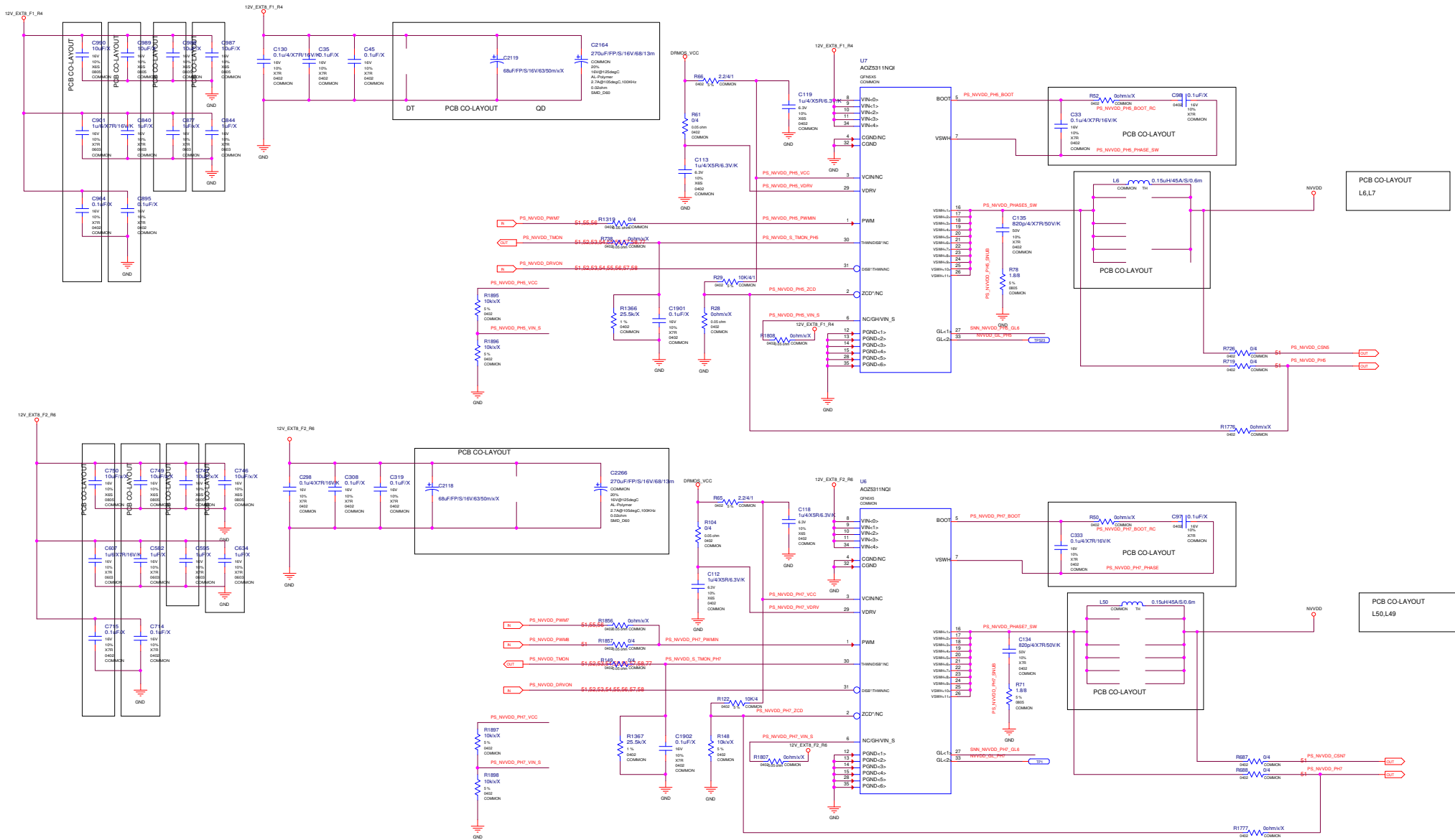
PS: NVVDD Phase 2 (PWM6)



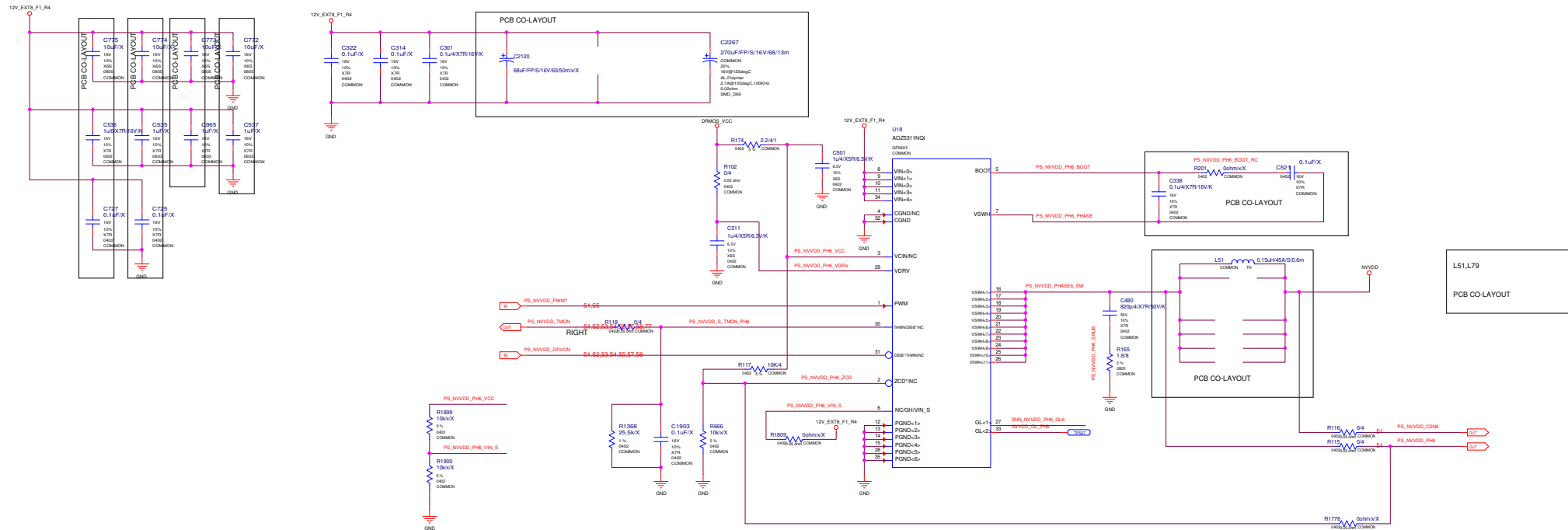
PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)

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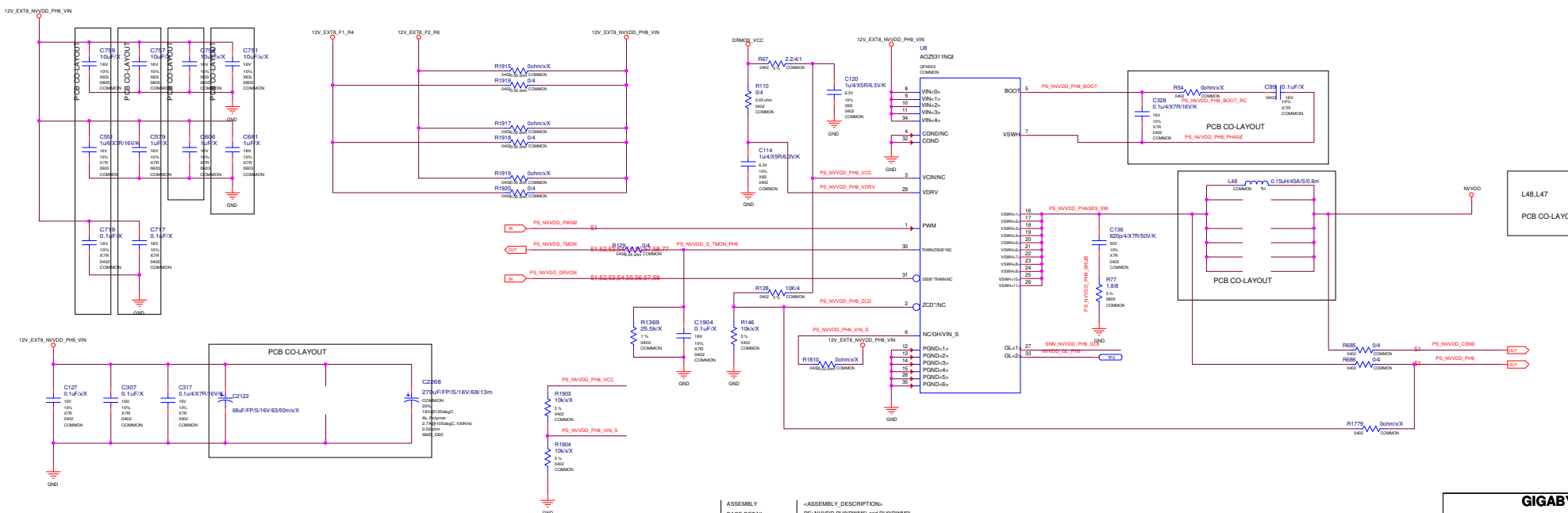
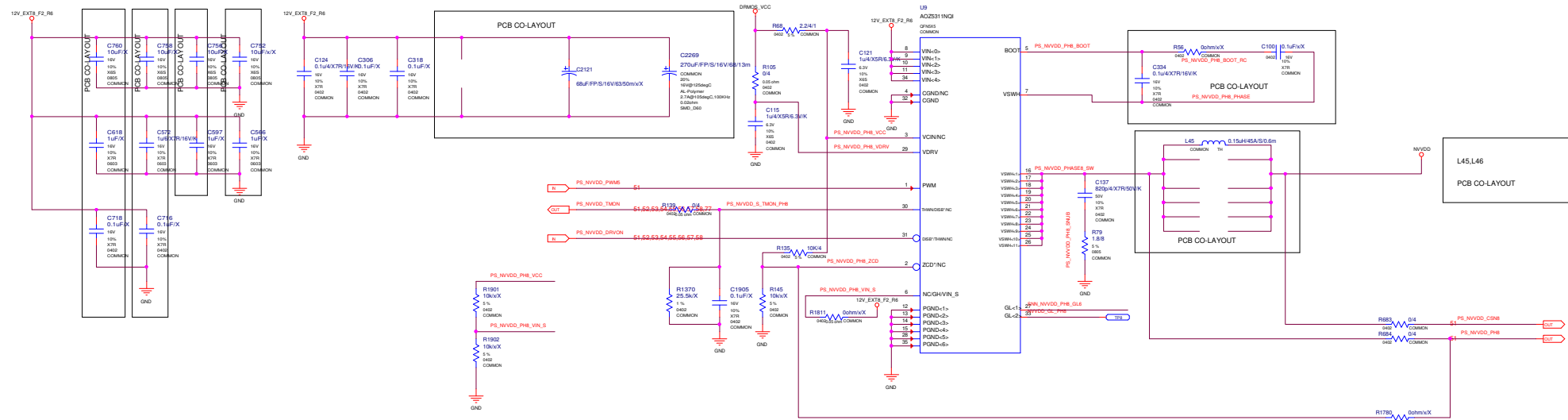
PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



PS: NVVDD Phase 6(PWM4)

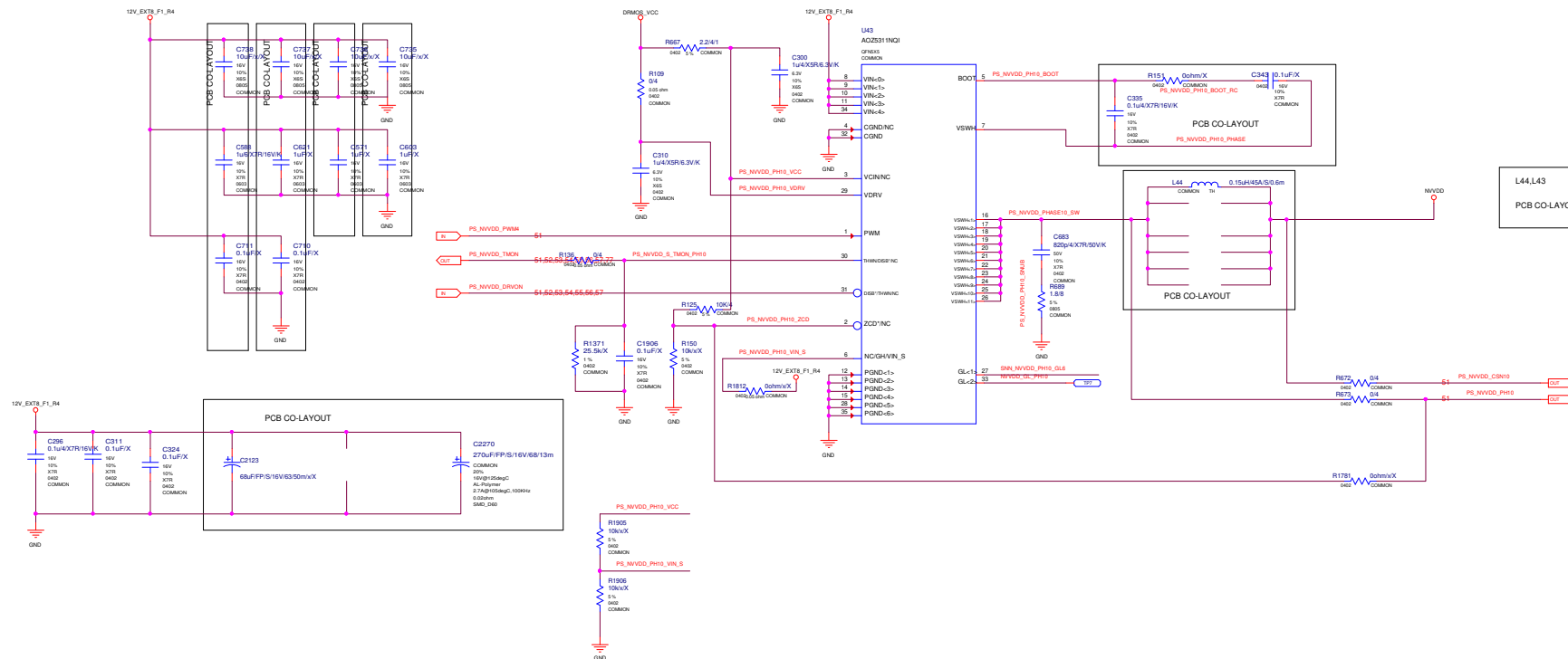


PS: NVVDD PH 8 (PWM5), PH 9(PWM2)



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PS: NVVDD Phase 10 (PWM7)



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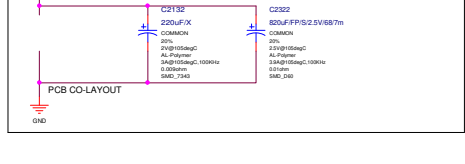
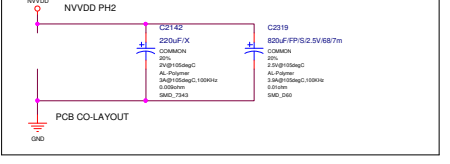
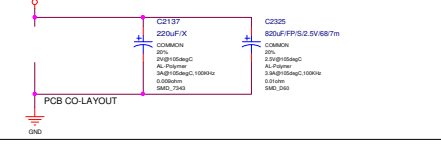
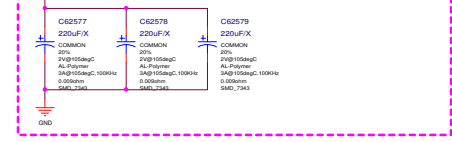
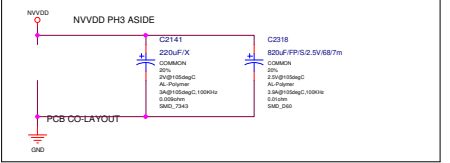
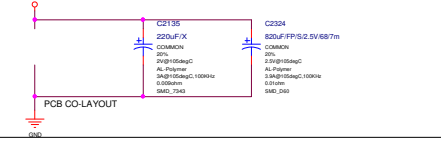
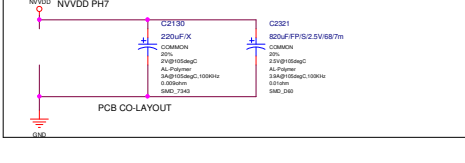
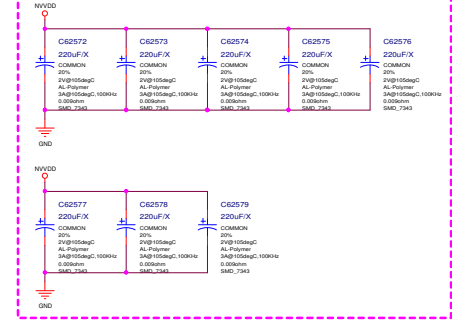
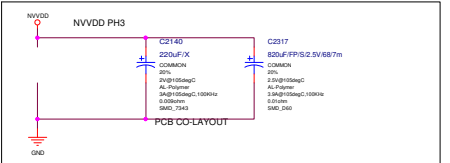
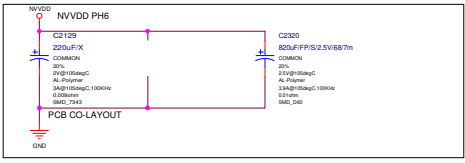
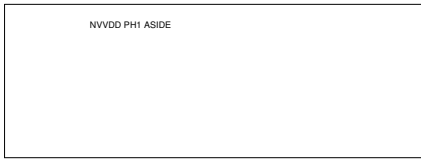
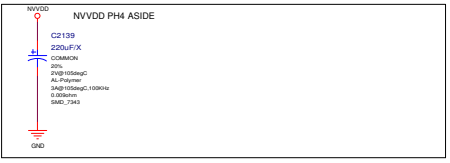
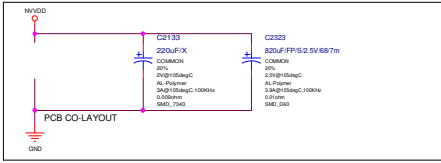
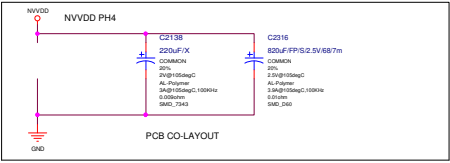
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| PCIE | | | |
| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | | Sheet 60 of 82 |

REFER TO PCB FOR BOM STUFFING



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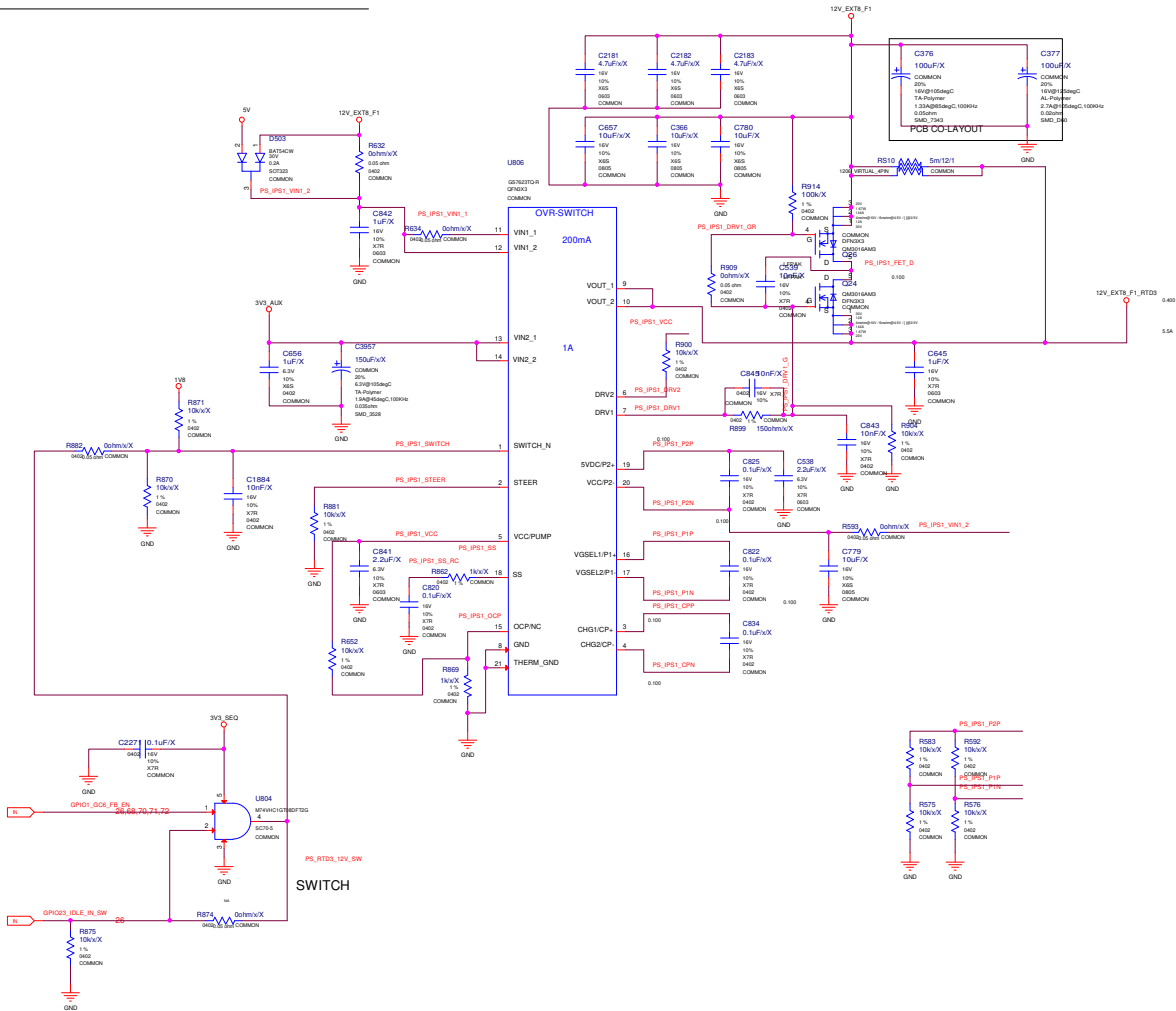
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| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | | Sheet 62 of 82 |

PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

| GPIO1 | GPIO23 | SWITCH | VOUT |
|-------|--------|--------|-------|
| 0 | 0 | 0 | 12V_F |
| 0 | 1 | 0 | 12V_F |
| 1 | 0 | 0 | 12V_F |
| 1 | 1 | 1 | 3V3A |



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PS: INPUT SWITCH RTD3
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GIGABYTE

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| Title | | | |
| PCIE | | | |
| Size | Document Number | Rev | |
| Custom | GV-N3090EAGLE-24GD | 1.0 | |
| Date: | Wednesday, September 30, 2020 | Sheet | 63 of 82 |

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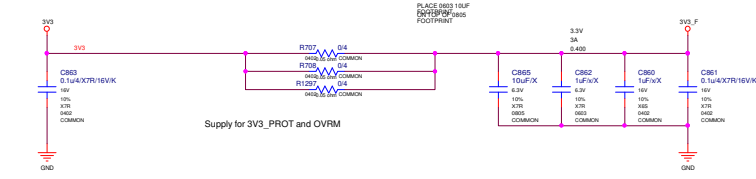
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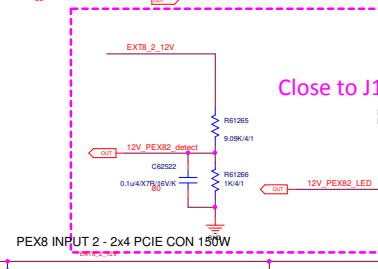
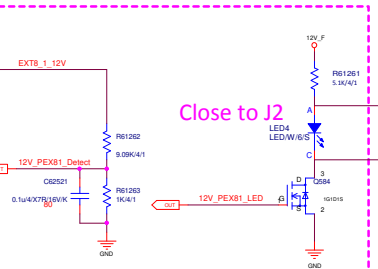
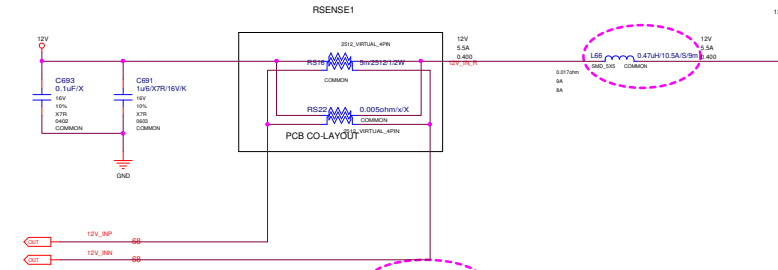
| GIGABYTE | | | |
|----------|-------------------------------|----------------|-----|
| Title | | | |
| PCIE | | | |
| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | Sheet 64 of 82 | |

PS: Inputs, Filtering, and Monitoring

PEX 3V3 INPUT - 10W

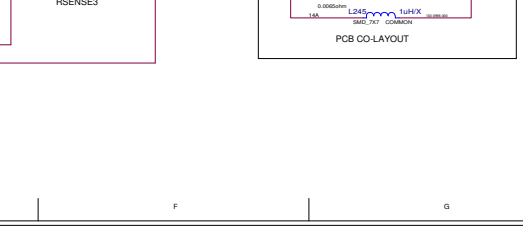
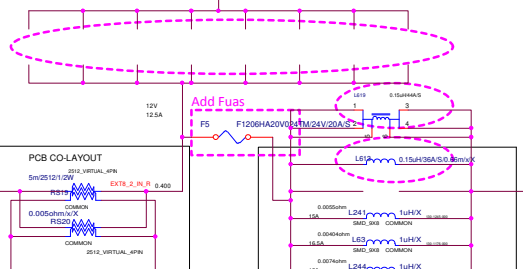
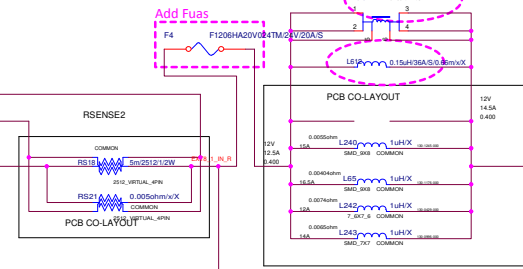


PEX_12V INPUT - 66W



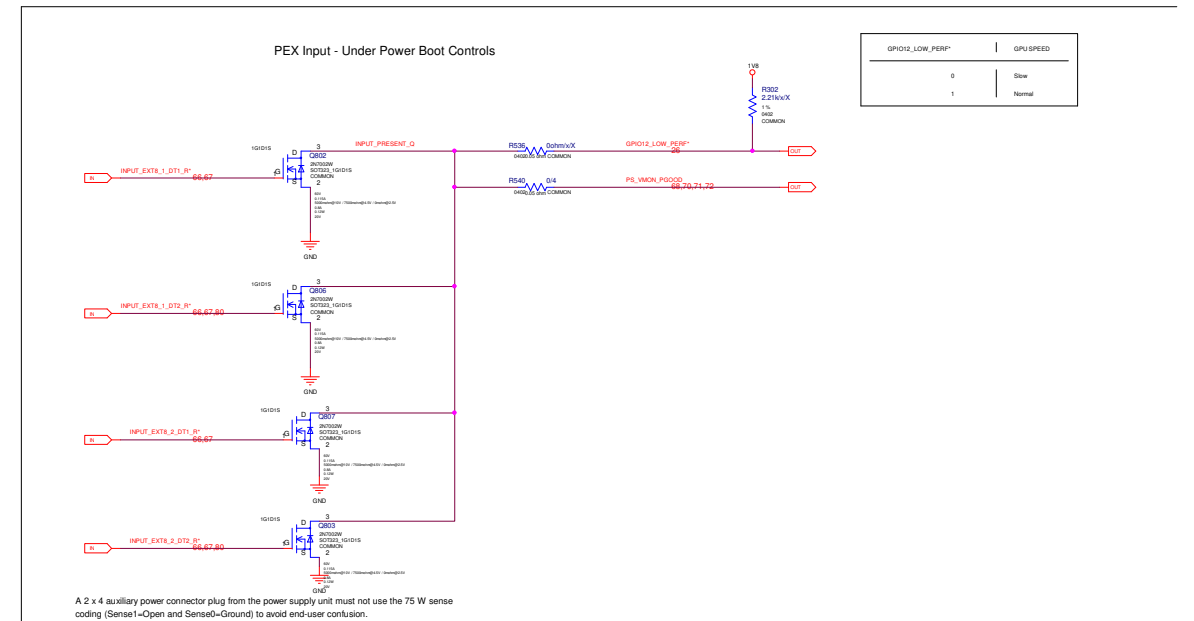
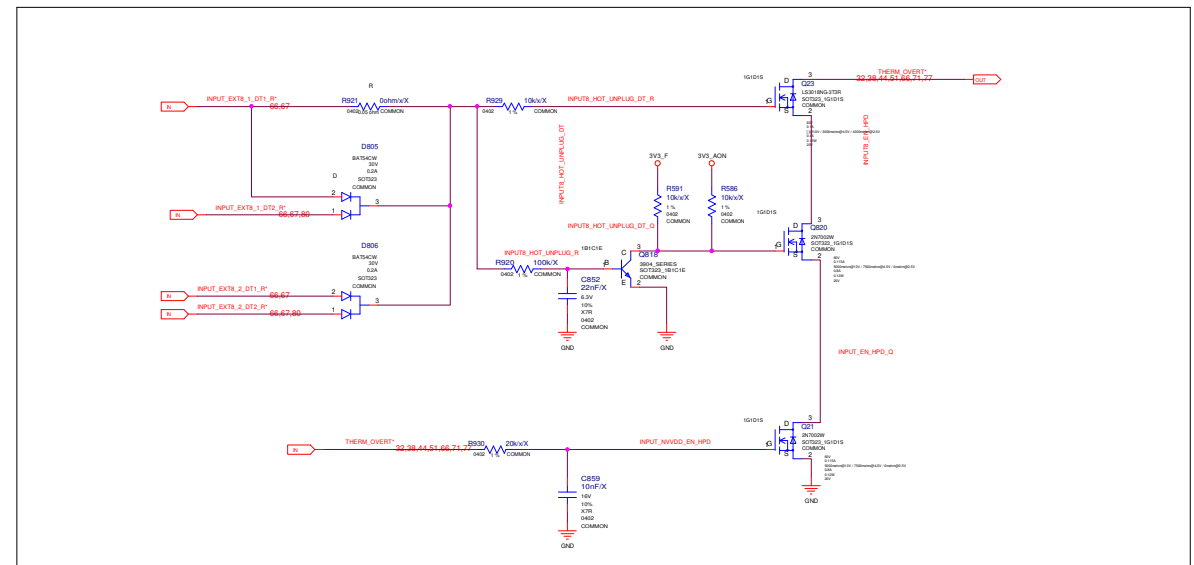
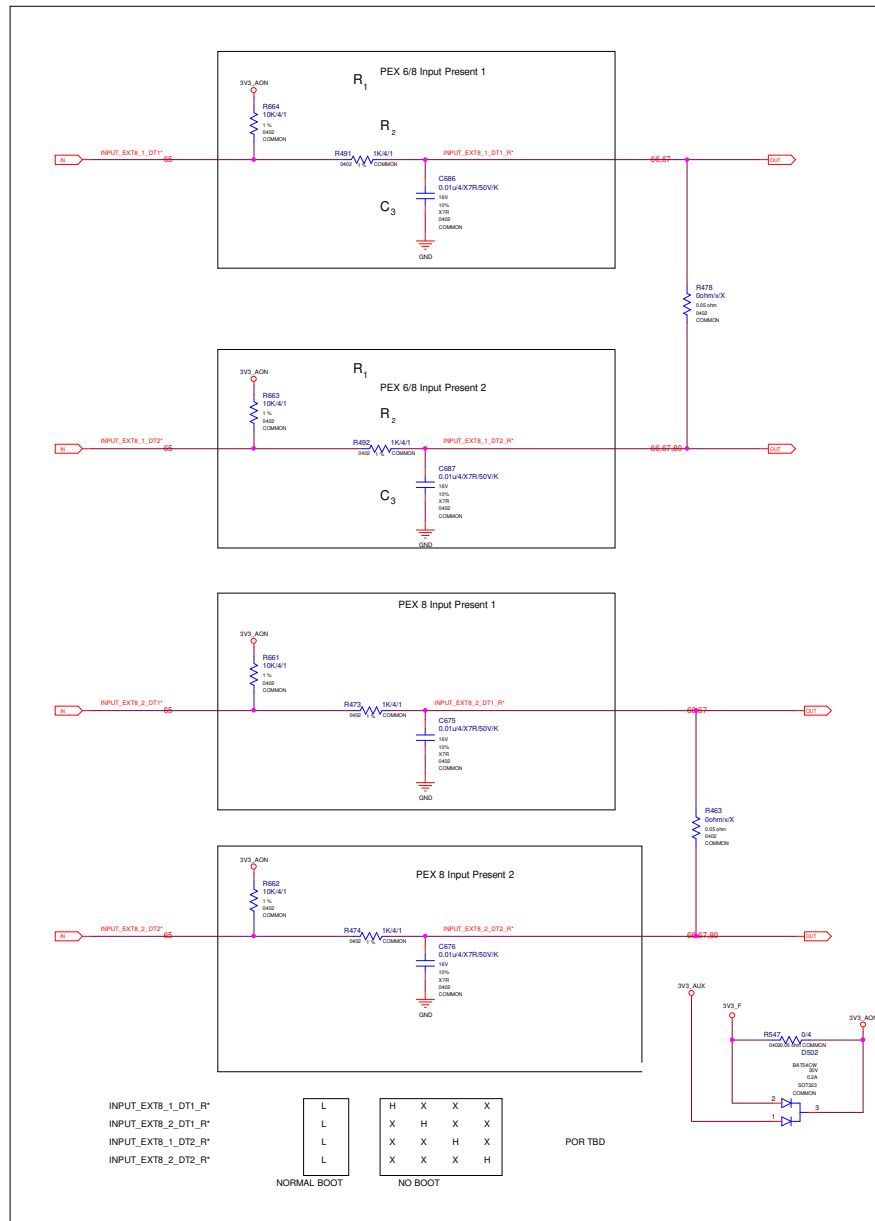
Close to J5011

Close to J5012



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PS: 12V Current Steering & Hot Unplug Detect

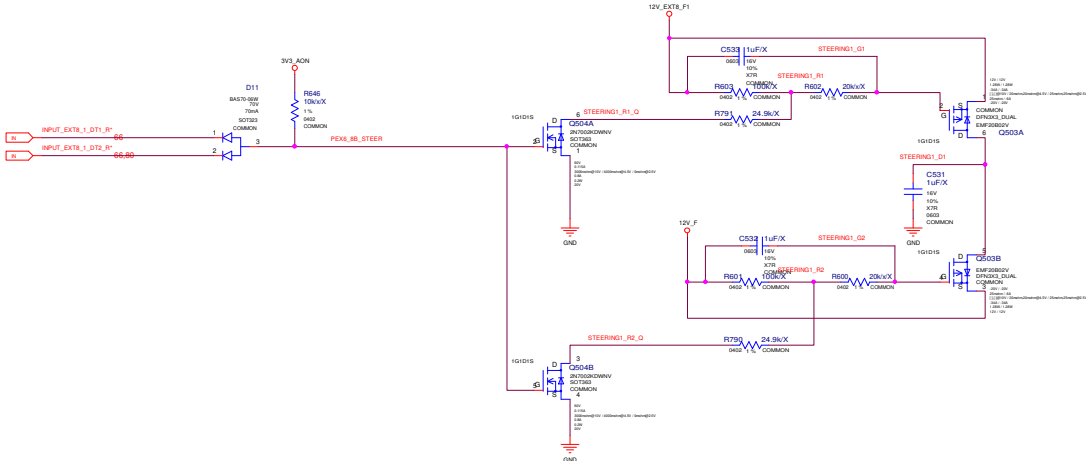


A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

PS: Discrete Steering

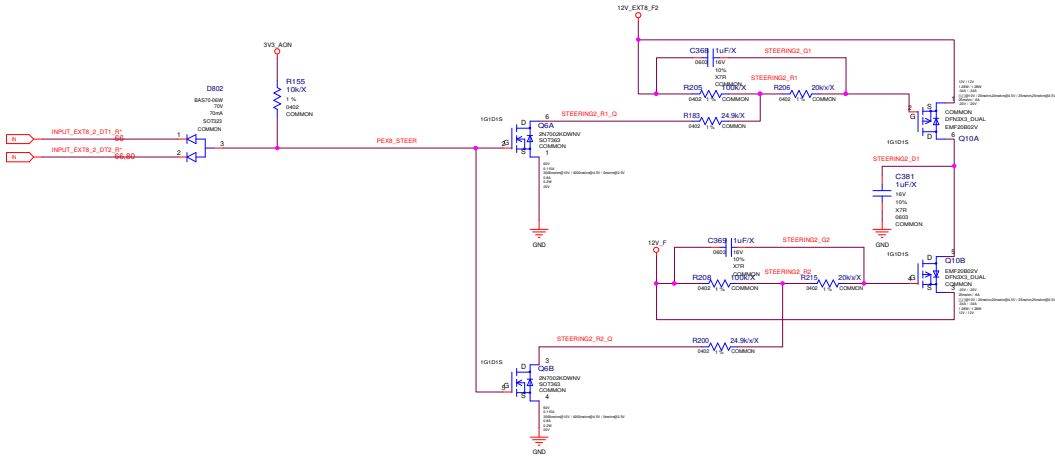
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

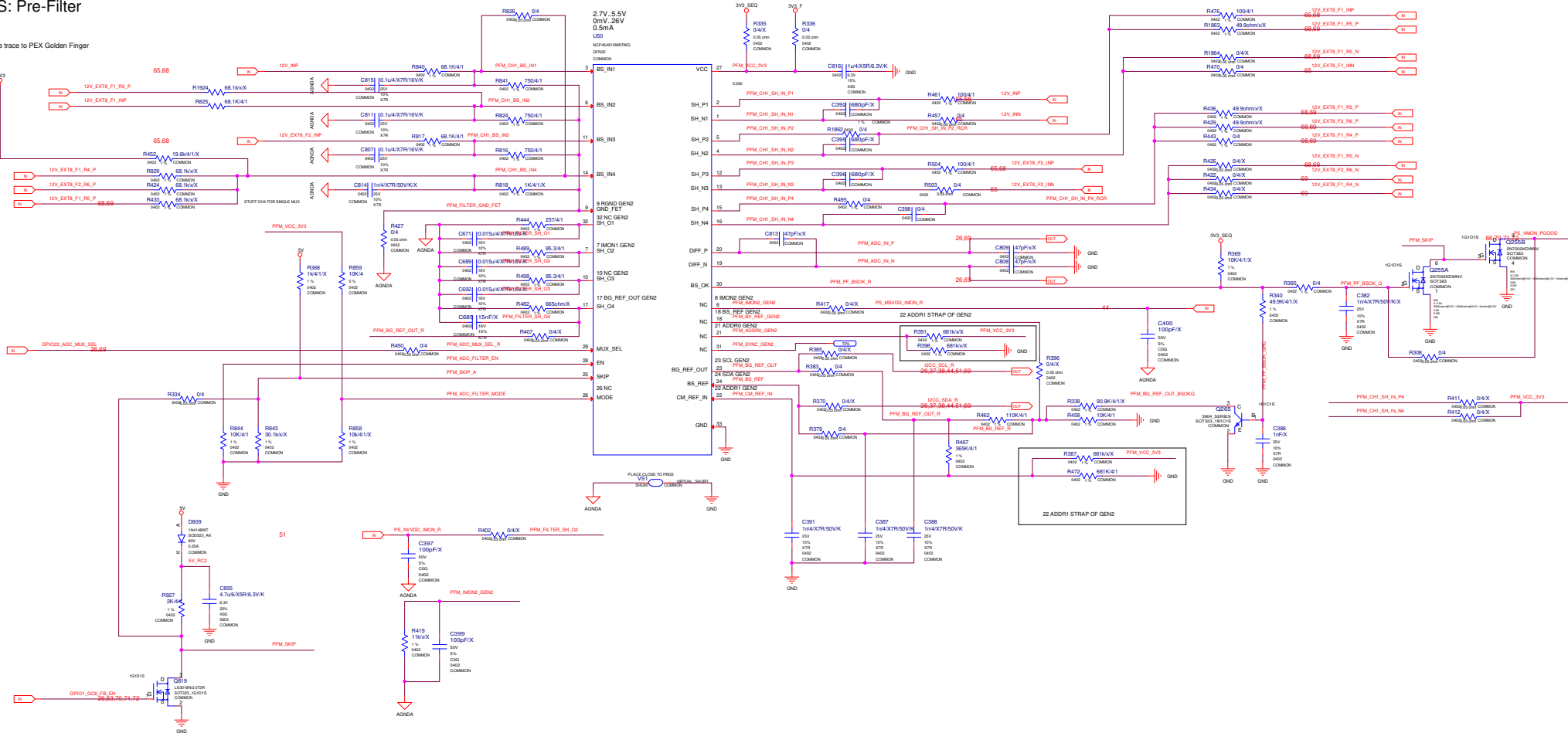
PEX12V AND 12V_EXT8_F2



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PS: Pre-Filter

Route the trace to PEX Golden Finger

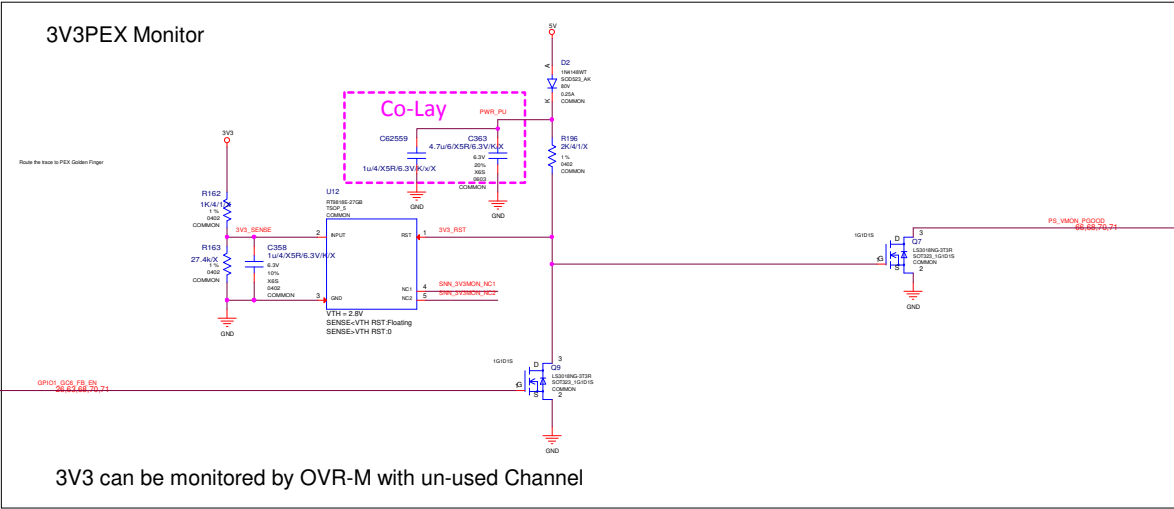


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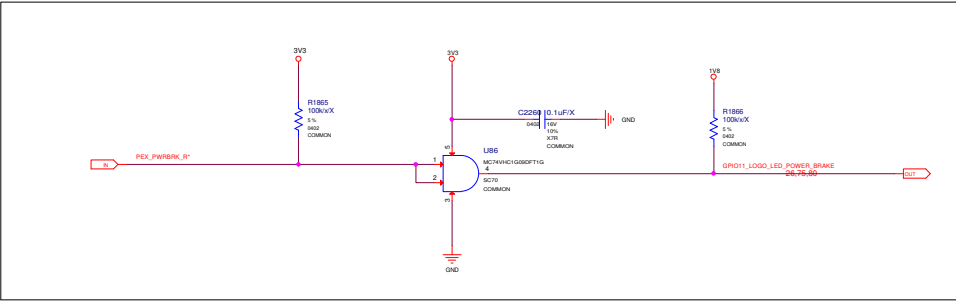
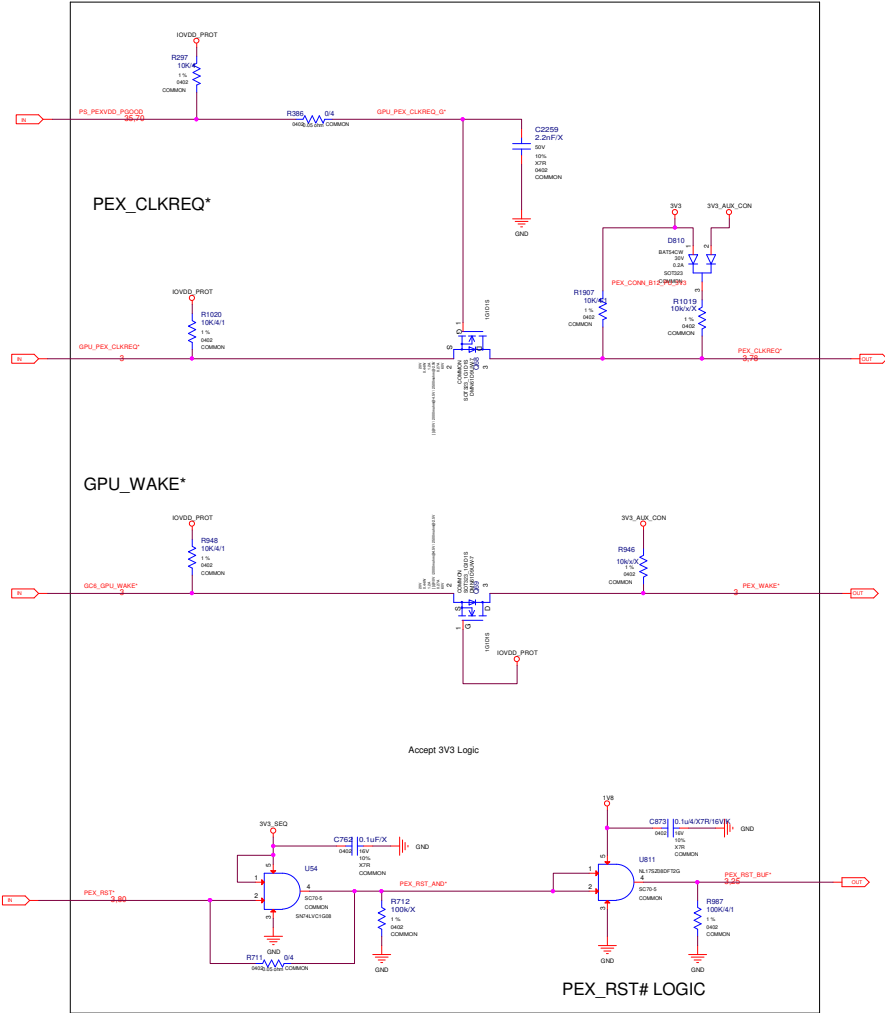
GIGABYTE

| | | | |
|--------|-------------------------------|-------|----------|
| Title | | | |
| PCIE | | | |
| Size | Document Number | Rev | |
| Custom | GV-N3090EAGLE-24GD | 1 | |
| Date: | Wednesday, September 30, 2020 | Sheet | 68 of 82 |

Sequence: 3V3 MONITOR



SEQUENCE:MISC

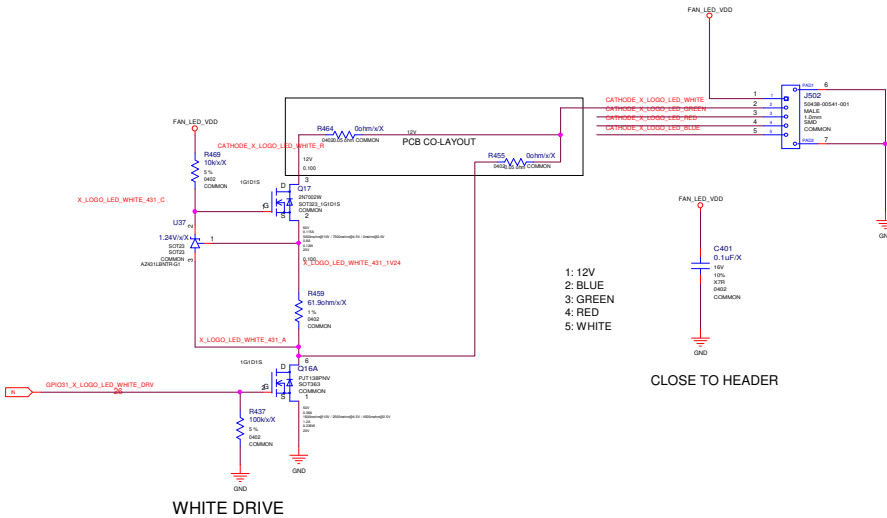


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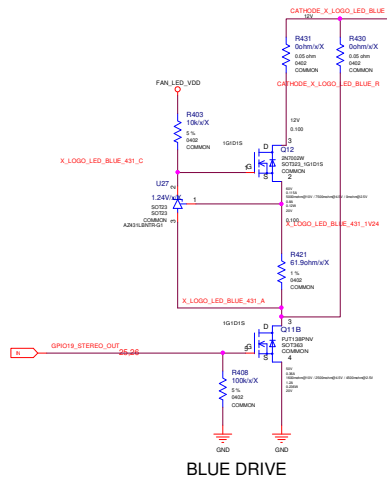
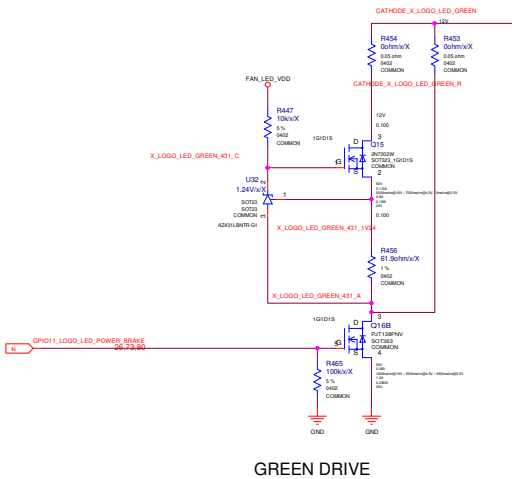
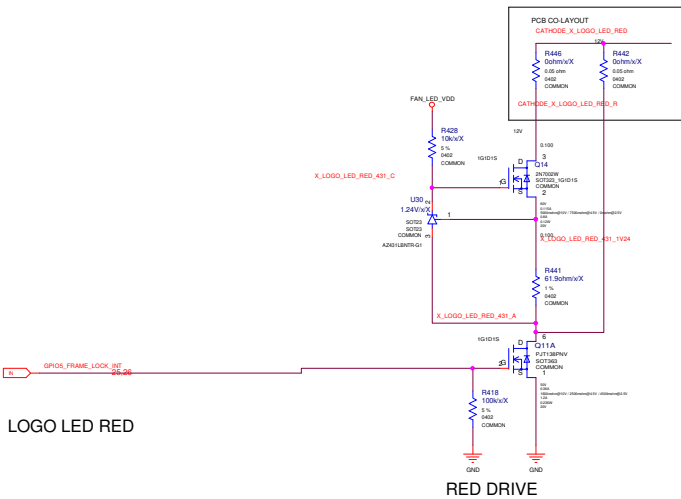
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| GIGABYTE | | | |
|----------|-------------------------------|--|----------------|
| Title | | | |
| PCIE | | | |
| Size | Document Number | | Rev |
| Custom | GV-N3090EAGLE-24GD | | 1.0 |
| Date: | Wednesday, September 30, 2020 | | Sheet 73 of 82 |



CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.

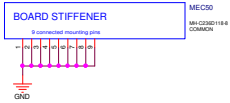


Mechanical: Mounting holes

BK up



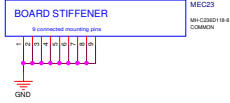
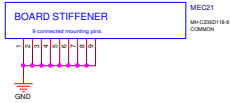
BK low



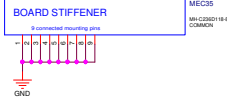
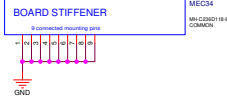
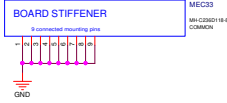
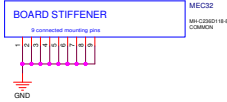
GPU



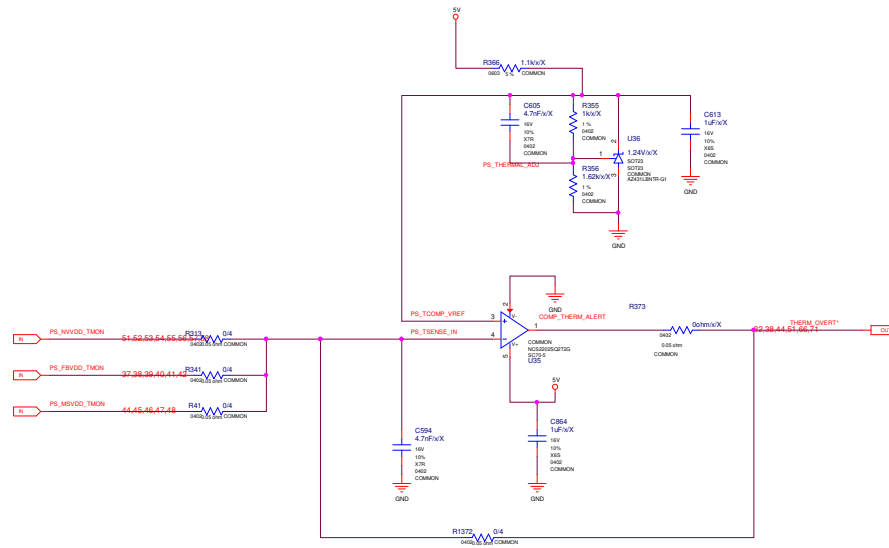
MOS



Backplane



VR THERMAL PROTECTION

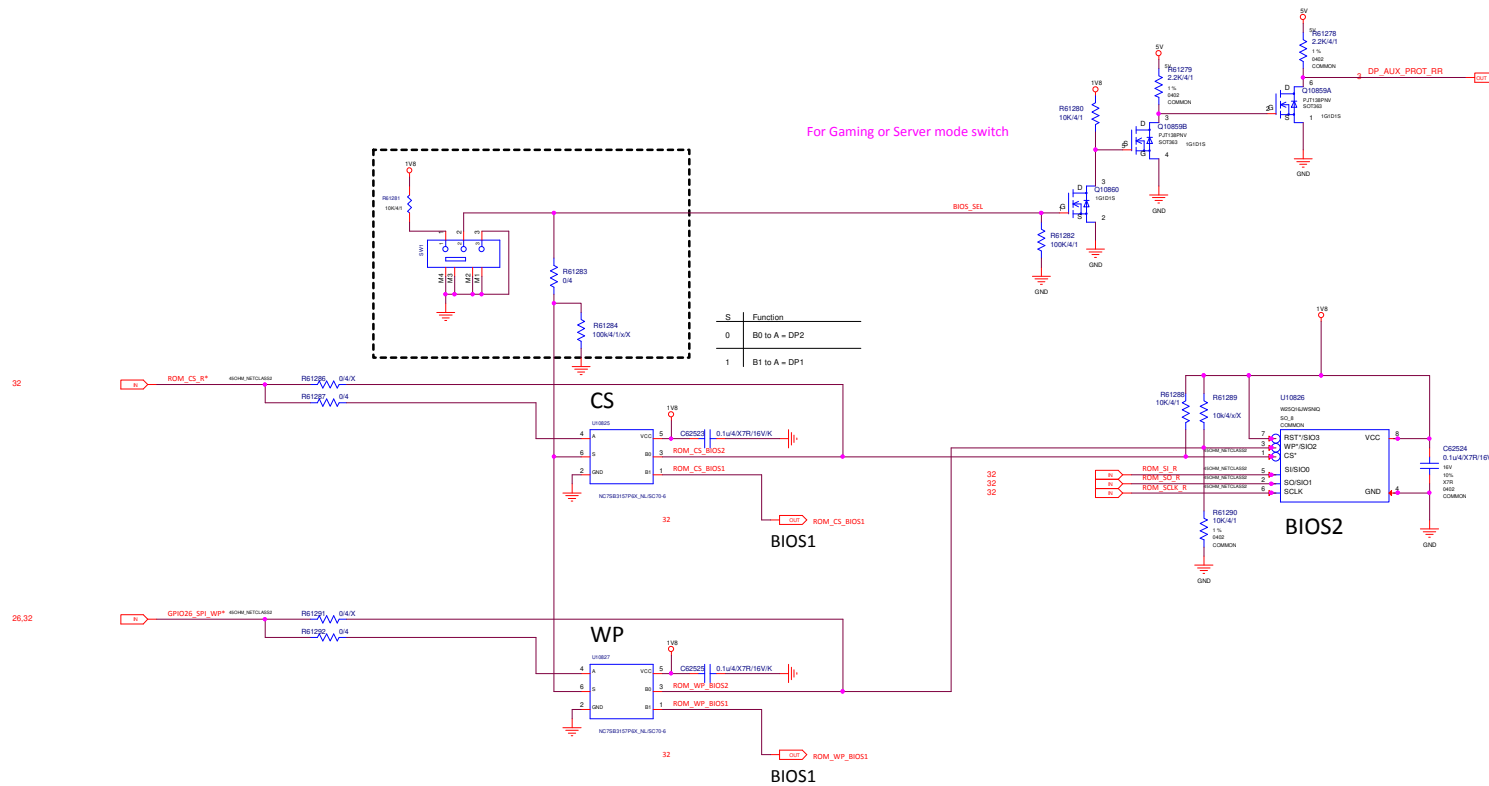


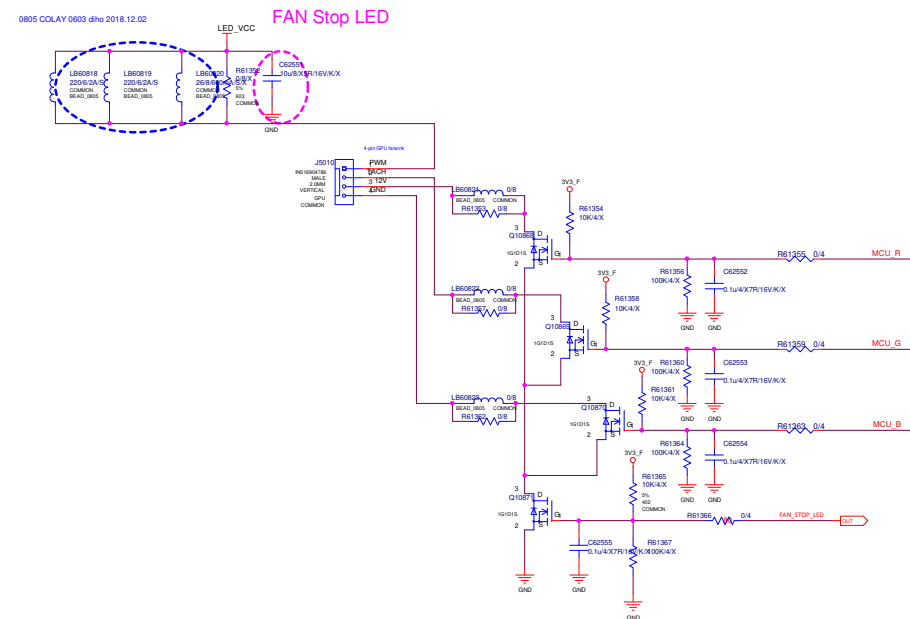
PCI TERM



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BIOS Switch





History

| Date | Modify |
|------------|---------------|
| 2018.07.21 | First version |